A high pulse naturally commutated static VAr compensator

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List of principal symbols and abbreviations

GENERAL

α	firing angle of the NC-SVC or TCR
α_{mt}	max. firing angle for single commutation mode
μ	general commutation interval of all bridges
μ_M	commutation interval of main convertor
μ_{R1} μ_{R2}	commutation interval of reinjection bridge
ω	angular frequency
AVR	automatic voltage regulator
B_1 B_2 B_{RJ}	thyristor bridges
C or (C_1 and C_2)	capacitance of the blocking capacitors
FACTS	flexible ac transmission system
HVDC	high voltage direct current
K_e	relation between commutating reactance and commutating resistance
L_{DC}	inductance of the dc reactor
N_M	main transformer turns ratio
N_R	reinjection transformer turns ratio
NC-SVC	naturally commutated static VAr compensator
p	pulse number
PLL	phase lock loop
pu	per unit
Q	compensator reactive power rating
R	all resistances inherent in the circuit lumped onto the dc side
S	VA rating of a transformer
SMES	superconducting magnetic energy storage
SVC	static VAr compensator
t	time
T_1 T_2 T_S	thyristors in the reinjection bridge

TCR	thyristor controlled reactor
TCT	thyristor controlled transformer
TF_M	main convertor transformer
TF_{RJ1} TF_{RJ2}	reinjection transformers

CURRENT

I_{DC}	36-pulse dc current
I_{RJ}	reinjection current the reinjection bridge
I_1	magnitude of the fundamental ac current
I_n	magnitude of the n^{th} harmonic in the ac current
I_{mt}	maximum ac current in the single commutation mode
I_{RMS}	phase current (RMS) at the main transformer secondary
$I_{RMS(F)}$	phase current fundamental (RMS) at the main transformer secondary
I_{SC}	short circuit current at the main transformer secondary
I_S, or ($I_{S(R)}$, $I_{S(Y)}$, $I_{S(B)}$)	Compensator currents
I_{S1}, or ($I_{S1(R)}$, $I_{S1(Y)}$, $I_{S1(B)}$)	ac currents in the star secondary windings of the main transformer
I_{S2}, or ($I_{S2(R)}$, $I_{S2(Y)}$, $I_{S2(B)}$)	ac currents in the delta secondary windings of the main transformer

VOLTAGES

V_1	phase to phase voltage at the main transformer secondaries
V_R V_Y V_B	ac supply voltages (ph-N) (this is modified with the 'prime' symbol to indicate different points in the circuit)
V_{DC}	36-pulse dc voltage
V_{B1} V_{B2}	bridge dc voltages in the main convertor
V_{RJ}	combined output of the reinjection transformer secondaries
V_C	voltage across the blocking capacitors

REACTANCES

X_T	supply and main transformer leakage
X_S	main transformer star secondary leakage
X_D	main transformer delta secondary leakage
X_{RJ}	reinjection transformer leakage
X_{MC}	total commutating reactance of the main bridge
X_{RC}	total commutating reactance of the reinjection bridge

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Publications associated with this thesis

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Brough, R.D., Arrillaga, J. and Duke, R.M. (1995) "Operation of a high-pulse ac/dc converter as a VAr compensator" European Power Electronics conf. (EPE), Sevilla, Spain, 19-21 Sept., Vol 2, pp 528-533.

Abstract

A new static VAr compensator (SVC) topology suitable for high voltage ac systems is proposed. This high pulse naturally commutated SVC is based on the ability of the ac/dc naturally commutated converter to regulate the absorption of reactive power and a novel method of achieving high pulse operation (i.e. with the dc ripple reinjection scheme).

Steady state and dynamic operating performance of the scheme are tested in a variety of ac system conditions with the help of two models techniques, a scaled down equivalent in hardware and a high voltage representation in a computer simulation package (EMTDC-PSCAD).

There is a linear relationship between firing angle and reactive current, and the 36-pulse harmonic characteristic of the compensator current is consistantly maintained over this operating range and in a variety of ac system conditions. Its dynamic performance is compared to that of the thyristor controlled reactor (TCR), when operating in the same power system environment, showing that the proposed scheme's voltage control ability is consistently faster than the TCR.

The main difference in the compensator performances, however, is the proposed scheme's inherent temporary overload capability. This difference shows that there is the opportunity for the proposed scheme to supersede the TCR technology and further work to clarify the compensator's viability is considered to be worth while.

Chapter 1

Introduction

At the turn of the 20th century some of the first commercial ac power transmission systems were being implemented to connect remote energy sources to load centres (Mershon, 1907). Supplying reactive power from the generating plant significantly limited transmission efficiency and it was quickly realised that distributed VAr control would improve the situation. Thus, synchronous condensors and switched/fixed shunt capacitors began to be included throughout these systems (Baum, 1921; Dubey *et al.*, 1986). As the size of the ac systems increased and VAr capacitors, being low cost, become widespread, while synchronous condensors, having a high cost, were typically located where their controllability/overload capability would best be used to provide emergency voltage support (Miller, 1982). Increasing economic and operational demands, however, showed the shortcomings of the synchronous condensor and new cheaper compensators with better reliability and better dynamic response were in demand (Gavrilovic, 1973).

A large part of the synchronous condensor cost arises because of its rotating parts, resulting in consideration of static VAr compensators (SVC) as an alternative. One of the first SVCs that was widely implemented was the saturable reactor. It gives improved dynamic performance, but its voltage control behaviour is defined by the magnetic properties of the reactor core and the interconnection of reactor windings, giving poor control flexibility (Miller, 1982). In the 1970s the power thyristor reached a point where it could viably control high levels of power and the thyristor switched capacitor/reactor, thyristor controlled reactor (TCR) and thyristor controlled transformer (TCT), which is a derivative of the TCR, were developed (Miller, 1982; Frank *et al.*, 1981; Petersson *et al.*, 1993). Even though the TCR (or TCT) normally lacks overload capability and generates compensator current harmonics, it provides a significant improvement in control flexibility over the saturated reactor. Moreover,

it has lower cost, lower maintenance and improved response time over the synchronous condensor (Engberg *et al.*, 1979; Ainsworth *et al.*, 1980; Hanson, 1985; Becker, 1991), making it the predominant choice for "high performance" VAr compensation.

In recent years the use of solid state switches to control power flow in the ac system has been generalised into a concept called the flexible ac transmission system, or FACTS (Hingorani, 1991), of which the SVC is an important part. With the advent of the FACTS concept there is significant interest in the development of new SVC topologies that may improve the economic and technical performance. Present SVC research tends to favour forced commutated topologies because of their increased controllability, as compared to thyristor based options, providing capabilities such as two quadrant operation (Sumi *et al.*, 1981; Eunson *et al.*, 1992; Hingorani *et al.*, 1993; Gyugyi, 1994). This technology, however, is still in its infancy and it will be many years before it is in common use (Le Du *et al.*, 1992; Chamia *et al.*, 1990). In the interim, the search continues for new compensator topologies that utilise reliable and tested components.

It has been mentioned by Gyugyi (1976) and investigated by Arrillaga *et al.* (1982) that the ac/dc convertor can be dedicated to the control of reactive power and become a naturally commutated SVC (NC-SVC). Other instances of naturally commutated ac/dc convertors being used for VAr control occur in applications such as high voltage dc transmission (HVDC) (Christensen *et al.*, 1994) and Superconducting Magnetic Energy Storage (SMES) (Boenig *et al.*, 1981; Banerjee *et al.*, 1990). The primary goal for both HVDC and SMES is the control of active power, which places limits on the reactive power controllability, reducing effectiveness. Furthermore, the firing angle modulation (Banerjee *et al.*, 1990) and variable free wheeling (Boenig *et al.*, 1982) techniques, used to control the VArs, both increase the ac current harmonics.

One reason why the NC-SVC solution has not gained favour is because of the difficulty in eliminating the high levels of ac current harmonics associated with 6 and 12-pulse schemes. The two conventional harmonic elimination methods are pulse multiplication, via the interconnection of multiple Graetz bridges, and ac filters (Galloway, 1977; Moore, 1977; Hall *et al.*, 1990; Karady *et al.*, 1992). Both of these techniques make the low pulse NC-SVC uneconomical compared to existing compensator technology (i.e. TCRs).

An alternative method of pulse multiplication for ac/dc convertors was suggested by Baird *et al.* (1980), whereby a ripple reinjection scheme is added to a 6 or 12-pulse convertor to modify the its current and voltage waveforms and produce a high pulse convertor equivalent. Villablanca (1992) followed this work with a generalised analysis of arbitrary pulse multiplication for both parallel and series connected Graetz bridge configurations (e.g. 12-pulse increased to 24, 36 or 48-pulse etc.).

In this thesis the reinjection scheme is applied to the low-pulse NC-SVC to produce a high-

pulse NC-SVC and the latter is tested for competitiveness with existing compensator technology. Specifically, its viability has to be justified in terms of economic and operating characteristics, this thesis focusing on the latter. In particular, the interaction with the ac system, under both steady state and dynamic operating conditions are considered.

A limitation of the NC-SVC is that the reinjection scheme requires a convertor transformer(s) to operate. For the TCR, the transformer is usually omitted at low voltages because of its high cost, it is only needed when the higher ac voltages cause design problems in the thyristor assemblies. Thus, the proposed compensator is likely to be most competitive for high voltage and high power levels. At such power levels the 12-pulse convertor has proved the most economical solution and is therefore used as a basis for the proposed scheme. Moreover, the series connected Graetz bridge configuration is preferred over the parallel case because the latter has difficulties in maintaining balanced power sharing (Bennell, 1977). The level of pulse multiplication by the reinjection scheme depends on the difficulty of preventing unacceptable levels of harmonic distortion in the ac system. For the proposed scheme the pulse number is increased from 12 to 36, using a single reinjection bridge, in the anticipation that the remaining high order harmonics are easily eliminated.

In chapter 2 the theoretical steady state operation of the proposed scheme is considered, including a detailed description of the pulse multiplication process and the current control characteristics. Based on this ideal operation the ratings of the main components in the compensator are derived and this provides the means to estimate the proposed scheme cost against other topology options. However, more detailed construction information is needed before economic aspects of its viability can be explored fully and this is left for future work.

The theoretical operation in chapter 2 is tested by way of two modelling techniques: scaled down hardware and computer simulation, as illustrated in chapters 3 and 4, respectively. The hardware model, limited to steady state operation, is used to illustrate the effect the component values have on the compensator operation. The software model is capable of simulating both steady state and dynamic operation, and the latter requires the development of a suitable control scheme. A simple control scheme is chosen and its design is discussed in detail to clarify the dynamic results that follow.

In chapter 5 the power system implications of the compensator viability are considered. Steady state and dynamic interaction between the compensator and ac system are tested under various operating conditions. The controllability of the reactive current to compensate for ac voltage variations and the level of compensator current distortion are compared to those from an equivalently rated 12-pulse TCR, which is representative of current SVC technology.

Finally, general conclusions are discussed in chapter 6 and future work is suggested.

Chapter 2

The proposed scheme

The proposed scheme is a 36-pulse naturally commutated static VAr compensator (NC-SVC), consisting of a naturally commutated ac/dc convertor supplying an inductive dc impedance, as shown in figure 2-1 (Arrillaga *et al.*, 1982). In this case, the convertor is a series connected double Graetz bridge configuration (main bridges B_1 and B_2, and main transformer TF_M), called the main convertor, modified with a dc reinjection circuit that changes the 12-pulse conversion into 36-pulse (Baird *et al.*, 1980).

The reinjection scheme consists of two blocking capacitors (C_1 and C_2), which prevent dc voltage from appearing across the primary windings of the two reinjection transformers (i.e.

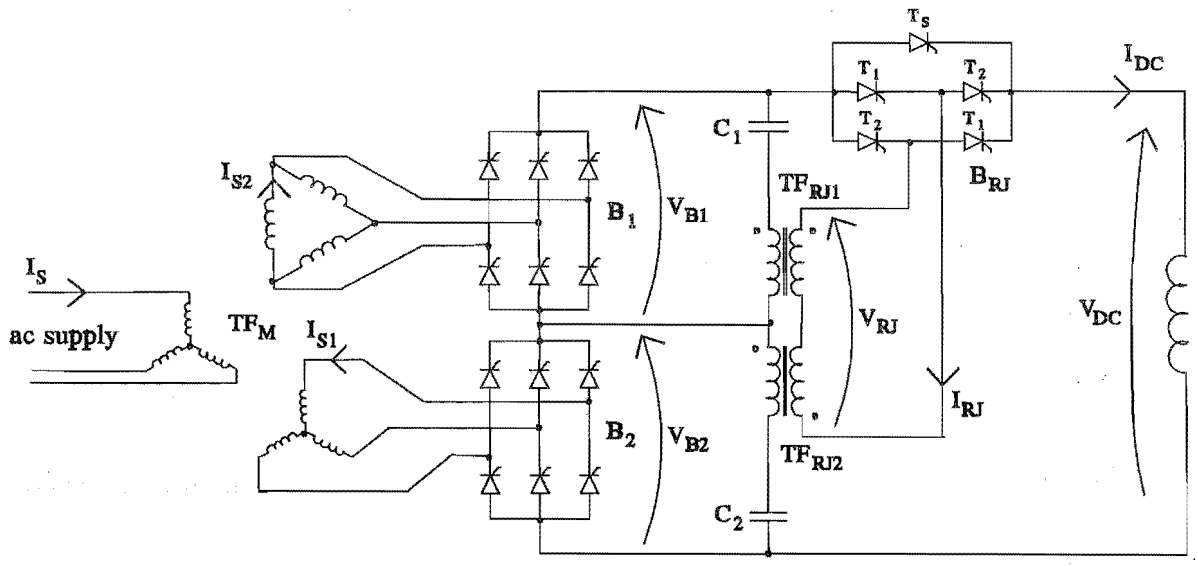

Figure 2-1: The 36-pulse naturally commutated SVC circuit.

the windings on the main convertor side of TF_{RJ1} & TF_{RJ2}) and a single-phase fully controlled naturally commutated bridge (thyristors T_1 and T_2) with a bypass switch (T_s), called the reinjection bridge (B_{RJ}).

Using theoretical operation as an illustration, the compensator is described further in this chapter. The steady state waveforms for the convertor are considered, along with the relationship between firing angle and compensator current. Furthermore, the component ratings are discussed by way of comparison with two alternative compensators to give an adequate frame of reference.

2.1 Convertor operation

The steady state convertor operation is defined in the following sections with respect to the conversion of ac to dc voltage and the conversion of dc to ac current.

2.1.1 ac to dc voltage conversion

Assuming that the phase to phase voltage at the main transformer secondary (V_1) has magnitude $1/\sqrt{2}$ and there are no commutation effects, the conventional 6-pulse dc voltage waveforms (V_{B1} & V_{B2}), that the two main bridges B_1 and B_2 produce, are shown in figure 2-2(a). Each 6-pulse dc voltage is applied to a series combination of blocking capacitor and primary winding of the reinjection transformer, so that only ripple appears across that winding and saturation is avoided. The secondary windings of the reinjection transformers are configured so that the ripple from V_{B1} and V_{B2} is subtracted and scaled (turns ratio N_R = 0.658). The resulting voltage, shown in figure 2-2(b), is periodically added in series with the 12-pulse dc voltage (V_{B1} +V_{B2}, shown in figure 2-2(c) as dotted lines) via the reinjection bridge and a 36-pulse dc voltage waveform is formed, shown in figure 2-2(c) as solid lines. Firing of the reinjection bridge thyristors are synchronised with the firings in the main convertor, as shown in figure 2-3. 10° after the main convertor changes state the shorting thyristor (T_S) conducts, removing the reinjection scheme from the circuit, shown in figure 2-2 as interval (2). This thyristor conducts for 10°, after which time either thyristors T_1 or T_2 are fired and the reinjection scheme is reconnected into the circuit, shown in figure 2-2(c) as intervals (1) or (3).

Villablanca (1992) states that, apart from the two times pulse multiplication case, where a single reinjection bridge with no shorting thyristor is used, the dc voltage modification is approximate. Measured from the waveforms in figure 2-2(c) the 12^{th} and 24^{th} harmonic in the 36-pulse dc voltage are 623 and 207 times smaller, respectively, than the 12-pulse

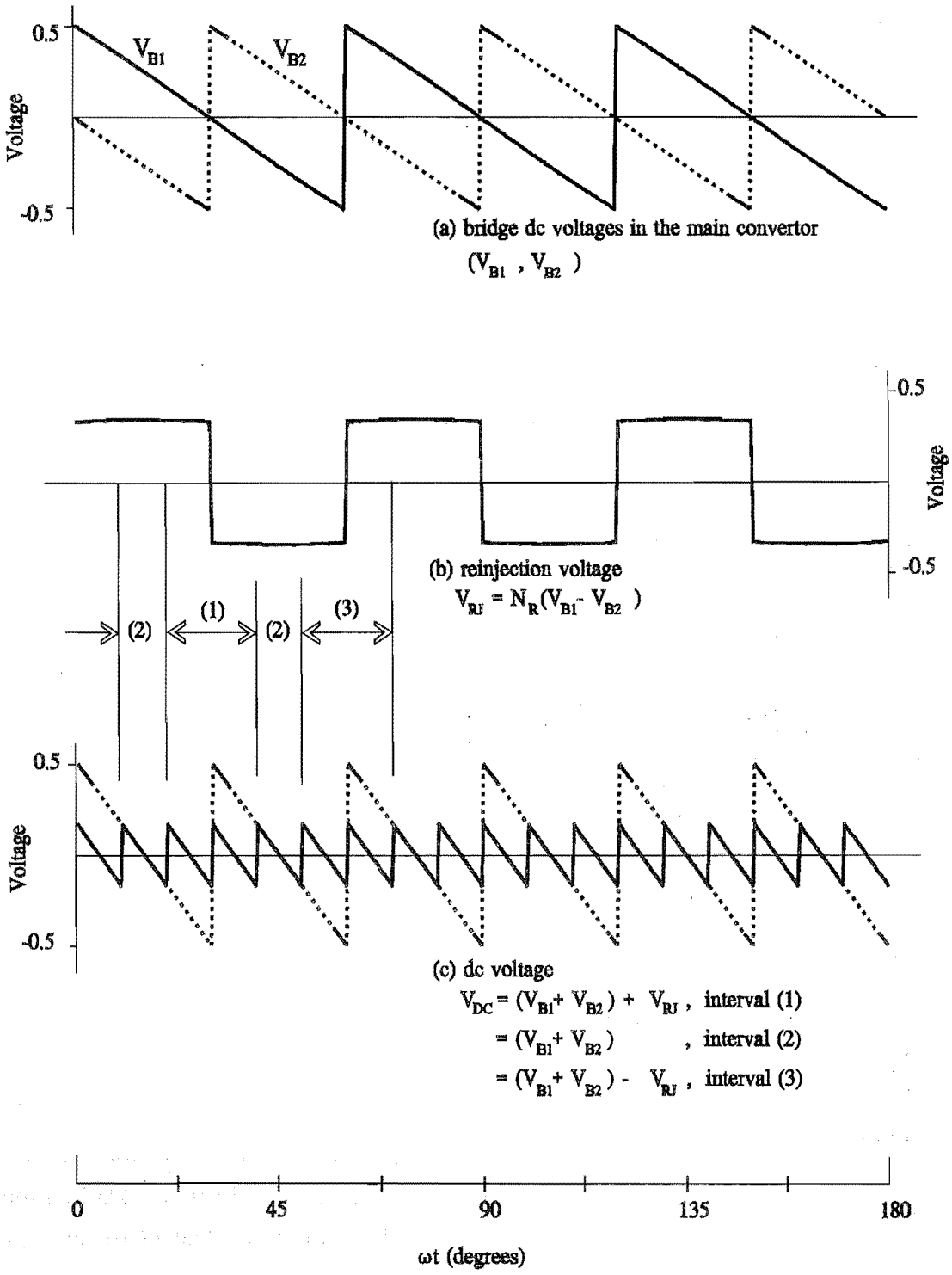

Figure 2-2: Theoretical voltage waveforms within the 36-pulse Naturally commutated SVC.

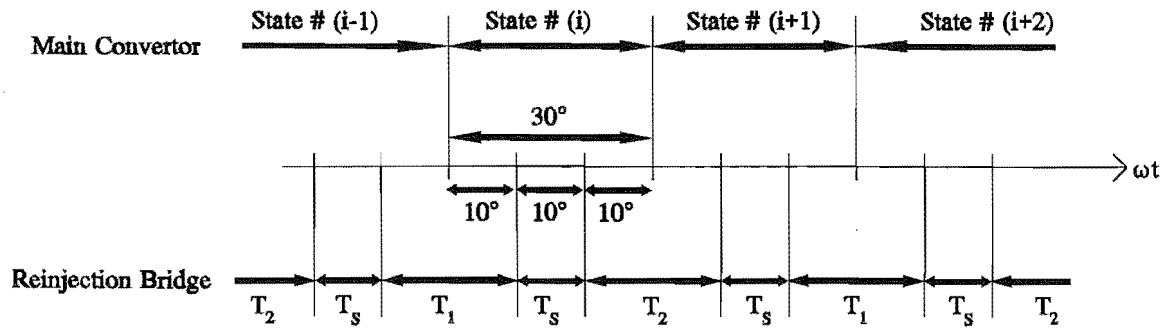

Figure 2-3: Thyristor switching pattern.

waveform. These harmonic magnitudes are minimum at 90° firing angle, which benefit the compensator because the compensator nominally operates near this angle, as discussed in section 2.2.

2.1.2 dc to ac current conversion

The reinjection bridge is in series with the dc circuit, where it periodically redirects the flow of dc current into the reinjection transformers in such a way as to produce a rectangular waveform (I_{RJ}) at six times the fundamental frequency (shown in figure 2-4(a)). This current, scaled by the reinjection transformer ratio (N_R), is injected into each main bridge and into the ac supply. As discussed in section 2.1.1, the reinjection bridge operation is synchronised with the main convertor. 10° after the main convertor changes state the reinjection scheme is bypassed and the reinjection current is zero. This lasts for 10° before reconnection.

The ideal waveforms shown in figure 2-4(b), (c) and (d) show the conventional 12-pulse waveforms drawn in dotted lines, while the solid lines represent the changes to the waveforms because of the reinjected current. In figure 2-4(b) and (c) the ideal currents in the secondary windings of the main transformer are shown. When these currents are added the ac supply current (I_S) is formed, as shown in figure 2-4(d).

In terms of harmonic content, the reinjection current contains harmonics with order 6n (where n=1,2,3,...). When reinjected into each main bridge the conventional harmonic distribution at the transformer secondary is modified as shown in figure 2-5. The relative phase and magnitude of the 12±1, 18±1, 24±1 and 48±1 harmonics in the reinjection current and conventional current are such that cancellation occurs. The 6±1 and 30±1 and 42±1 harmonics in the reinjection current, on the other hand, either have an equivalent phase or different magnitude to the conventional and the resultant harmonic magnitudes increase. In the case of the 36±1 harmonics, reinjection current levels are insignificant compared to the conventional and the harmonic magnitudes are effectively unchanged. When both main bridge

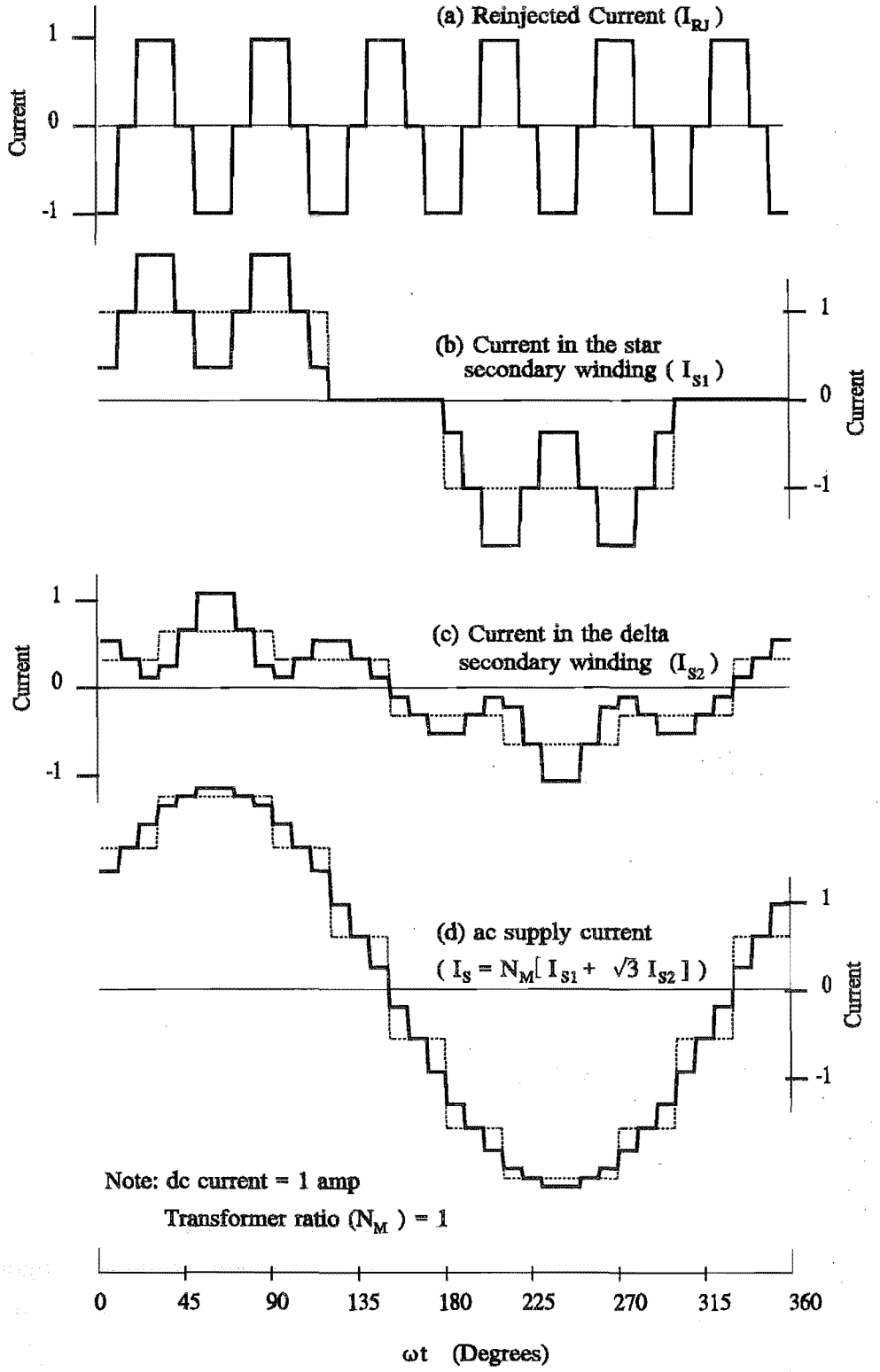

Figure 2-4: Theoretical current waveforms within the 36-pulse naturally commutated SVC.

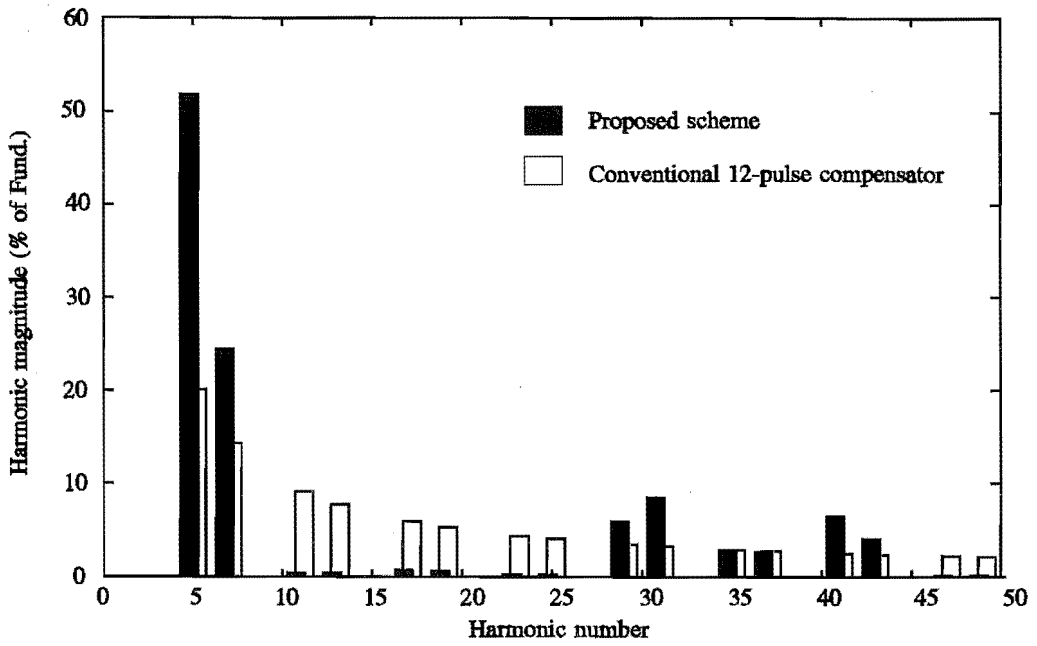

Figure 2-5: Harmonic content of the ac current in the main transformer secondary.

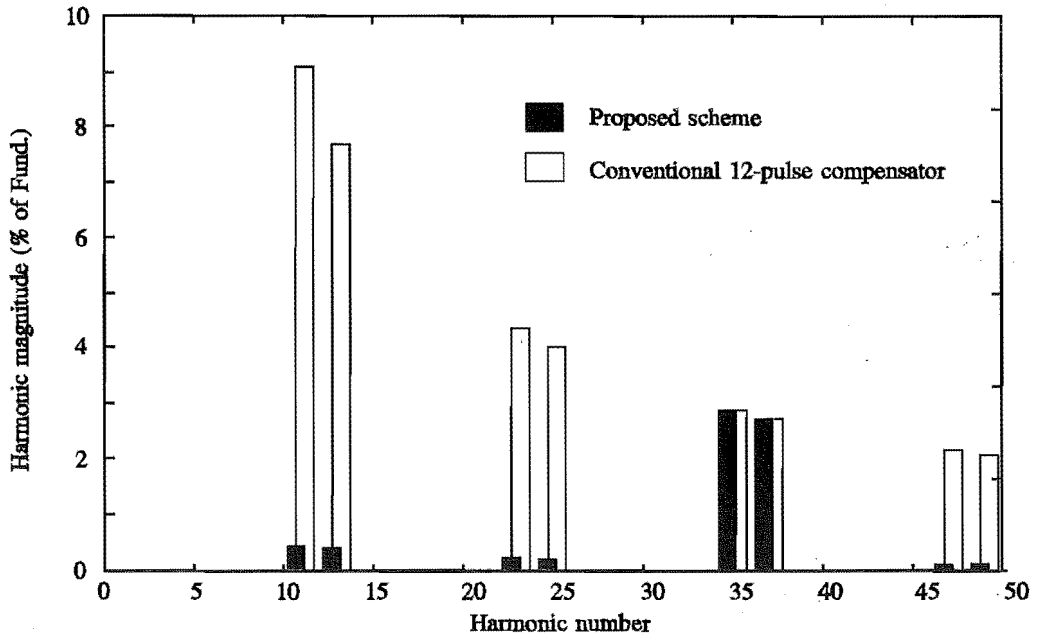

Figure 2-6: Harmonic content of the compensator's ac current.

currents are combined via the star-delta transformer configuration the 6(2n-1)±1 harmonics (where n=1,2,3,4...) are eliminated from the compensator current, as shown in figure 2-6. For the same reasons as discussed with the ac to dc voltage conversion, the dc to ac current conversion is approximate. This approximation is evident in that both the 12±1 and 24±1 harmonics are reduced by a factor of approximately 20, rather than being totally eliminated.

The consequences of not completely removing these harmonics are discussed in chapter 5 in the context of the ac system harmonic susceptibility.

2.2 Compensator operation.

The reactive current absorbed is directly related to the dc current (I_{DC}); by reducing the firing angle from 90°, the dc current can, ideally, increase indefinitely. In practice, the inductive impedances of the main transformer and ac system will increase the commutation overlap and eventually lead to simultaneous commutations on both of the main bridges, which constitute an effective short circuit. Short circuit at the main transformer secondary define the maximum compensator current that can be absorbed by the NC-SVC (I_{sc}).

The commutations not only limit the reactive current, but also change the harmonic distribution in the compensator current that are shown in figure 2.6. The ideal relationship between firing angle and the ac current fundamental (I_1) and harmonic (I_n) magnitudes are shown in figure 2-7. This figure is constructed assuming that the dc reactor is very large, the resistance inherent in all components does not affect the commutation of the switches and the commutation intervals of the main convertor are equal to that of the reinjection bridge.

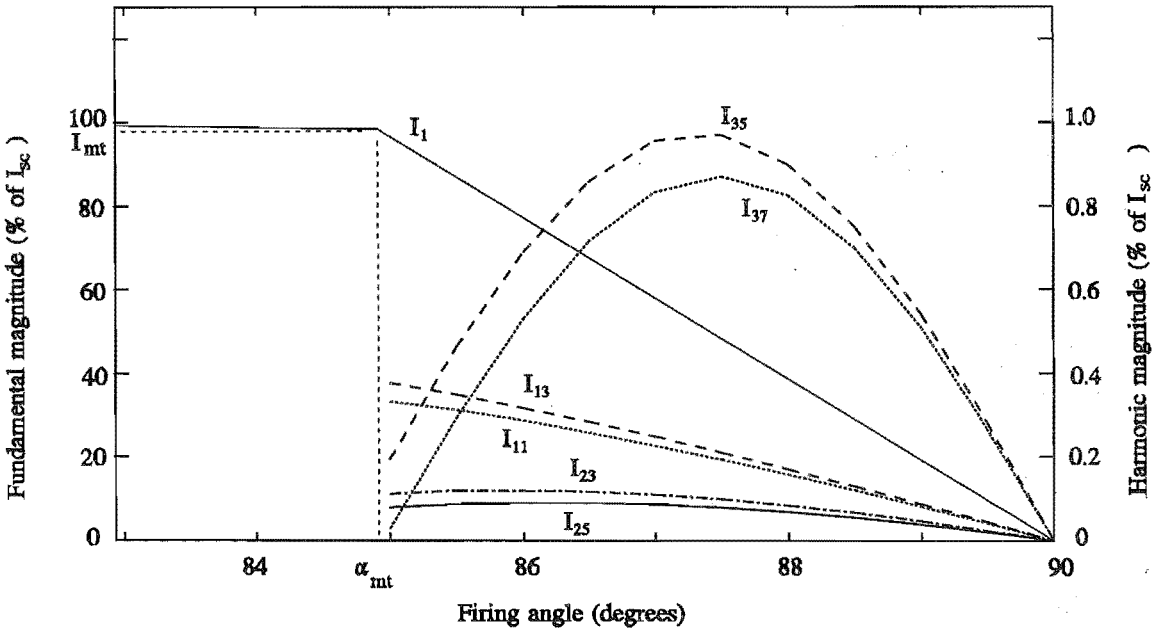

Figure 2-7: Steady state compensator characteristic with firing angle.

Two modes of compensator operation are identified: single commutation mode, where there is only one commutation occurring in any bridge at any one time, and multiple commutation

mode, where the main and reinjection bridge commutations overlap. In the single commutation mode, the fundamental current is zero at 90° firing angle and there is a linear increase in current as the firing angle is decreased. At a firing angle of α_{mt}, corresponding to a current level of I_{mt}, commutations overlap and the multiple commutation mode is entered. The reinjection circuit ceases to generate the required levels of current and the commutation intervals in the main bridges are significantly increased. Below α_{mt}, multiple commutations significantly limit the fundamental current increase, illustrated in figure 2-7 as an abrupt change in slope of the I_1 trace.

Figure 2-7 is constructed by first calculating the dc current level for a given firing angle. The convertor is represented as a dc voltage source ($\frac{6\sqrt{2}}{\pi}V_1\cos\alpha$, where V_1 is the phase to phase voltage magnitude at the main transformer secondary and α is the firing angle) in series with an equivalent resistance (K_eX_{MC}), as described by Kimbark (1971). The resistance represents the effects of all commutations in the convertor. It is related to the commutating reactance of the main convertor (X_{MC}) by the constant K_e, which is derived in section 2.2.1.

The convertor supplies a dc impedance, which, for steady state consists of a single resistance (R), being the sum of all the resistances inherent in all the components in the circuit. Both R and K_eX_{MC} limit the dc current (I_{DC}) according to

$$I_{DC} = \frac{\frac{6\sqrt{2}}{\pi}V_1 \cos\alpha}{K_eX_{MC} + R} \qquad \textbf{(2-1)}$$

Construction of the ac current from the dc magnitude includes the assumption that the commutation process is linear. All commutation intervals have the same duration and this value is calculated from the main bridge commutation. In the main bridges B_1 or B_2 the commutation is described by the conventional Graetz bridge commutation equation, as described by Arrillaga (1983). In this case, however, the effective dc current during the commutation process is reduced to $(1-N_R)I_{DC}$, therefore

$$\int_0^{(1-N_R)I_{DC}} dI_{S1} = \frac{1}{2X_{MC}} \int_\alpha^{\alpha+\mu} \sqrt{2}V_1 \sin(\omega t)\, d\omega t \qquad \textbf{(2-2)}$$

When equation (2-1) is substituted into equation (2-2) it can be shown that

$$\cos(\alpha)\left(1 - \frac{X_{MC}(1-N_R)\frac{12}{\pi}}{R + K_eX_{MC}}\right) = \cos(\alpha+\mu) \qquad \textbf{(2-3)}$$

The application of a Fourier transform to the output of the dc to ac current conversion process

results in the fundamental and harmonic magnitudes, which are displayed in figure 2-7 as a percentage of maximum current, i.e. I_{sc}.

2.2.1 The effective resistance of the commutation process

The analysis to calculate the effective resistance, because of the commutations in a conventional Graetz bridge (Kimbark, 1971), is adapted to the proposed scheme. The steps in the analysis are; to find the decrease in dc voltage because of each commutation, then find the average voltage decrease and relate it to the dc current via an expression for the commutation process, i.e. equation (2-2). In the proposed scheme there are three commutations to consider, as shown in figure 2-8. Over the 30° interval there is a main bridge commutation in interval 1 and two reinjection bridge commutations (called commutations 1 and 2, respectively) in intervals 3 and 5, of duration μ_M, μ_{R1} and μ_{R2}, respectively.

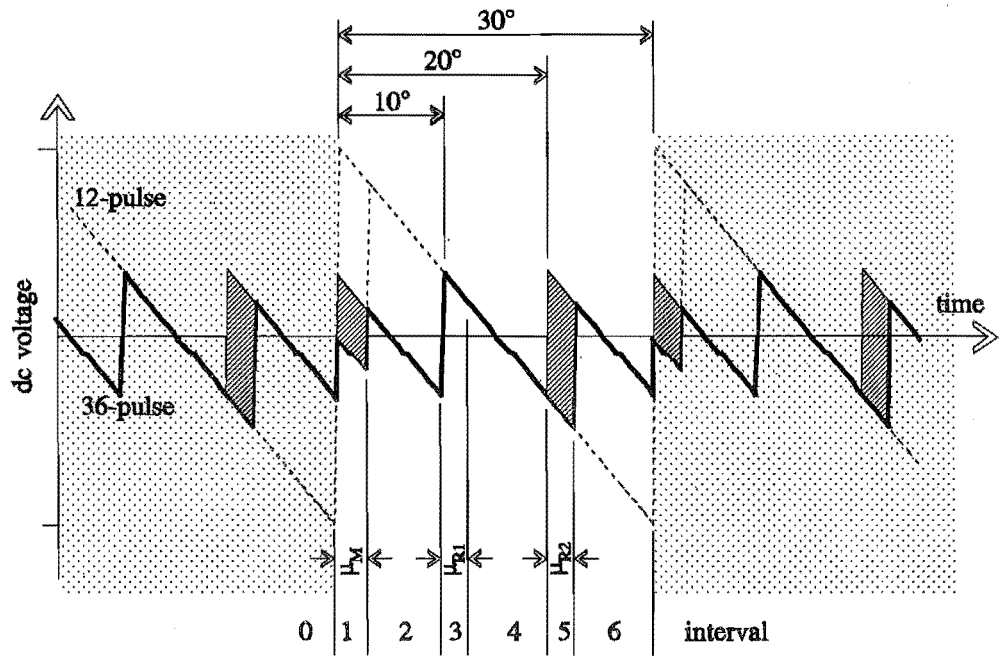

Figure 2-8: Theoretical dc voltage waveforms when thyristor commutations are considered.

The instantaneous voltages during the various intervals are derived from the ac voltage sources (referred to the secondary side of the main transformer):

$$V_R = \frac{V_1}{\sqrt{3}} \angle 30°, \qquad V_B = \frac{V_1}{\sqrt{3}} \angle -90°, \qquad V_Y = \frac{V_1}{\sqrt{3}} \angle +150° \qquad (2\text{-}4)$$

The dc voltages for each main bridge (V_{B1} and V_{B2}) are defined as shown in table 2-1. As discussed in section 2.1.1 the 36-pulse dc voltage is constructed by adding and subtracting

voltages to portions of the 12-pulse dc voltage. Assuming that the blocking capacitor is large, at each interval this process is defined by

$$V_{DC} = V_{B1}(1+XN_R) + V_{B2}(1-XN_R) \qquad (2\text{-}5)$$

where X equals zero or ±1 depending on the conduction state of the reinjection bridge.

interval	V_{B1}	V_{B2}	X	V_{DC}
0	$V_Y - V_B$	$-\sqrt{3}\,V_B$		
1	$\frac{(V_Y + V_R)}{2} - V_B$	$-\sqrt{3}\,V_B$	-1	$\| = V_1\left(\frac{\sqrt{3}}{2}(1-N_R) + (1+N_R)\right)$ $\angle = 90°$
2	$V_R - V_B$	$-\sqrt{3}\,V_B$	-1	$\| = V_1\sqrt{(2+\sqrt{3}) + N_R^2(2-\sqrt{3})}$ $\angle = \tan^{-1}\left(\frac{2(1+N_R) + \sqrt{3}(1-N_R)}{(1-N_R)}\right)$
3	$\frac{(V_R - V_B) - \sqrt{3}V_B}{2}$	$\frac{(V_R - V_B) - \sqrt{3}V_B}{2}$	0	$\| = V_1\sqrt{2 + \sqrt{3}}$, $\angle = 75°$
4	$V_R - V_B$	$-\sqrt{3}\,V_B$	0	$\| = V_1\sqrt{2 + \sqrt{3}}$, $\angle = 75°$
5	$\frac{(V_R - V_B) - \sqrt{3}V_B}{2}$	$\frac{(V_R - V_B) - \sqrt{3}V_B}{2}$	0	$\| = V_1\sqrt{2 + \sqrt{3}}$, $\angle = 75°$
6	$V_R - V_B$	$-\sqrt{3}\,V_B$	+1	$\| = V_1\sqrt{(2+\sqrt{3}) + N_R^2(2-\sqrt{3})}$ $\angle = \tan^{-1}\left(\frac{2(1-N_R) + \sqrt{3}(1+N_R)}{(1+N_R)}\right)$

Table 2-1: Construction of the 36-pulse dc voltage.

From equation (2-5) the sinusoidal portions that make up the 36-pulse dc voltage are summarised in table 2-1. The decrease in the dc voltage during interval 1 because of the commutation of the main bridge is given by the difference between the interval 2 dc voltage minus that of interval 1, i.e. $V_1\frac{(1 - N_R)}{2} \angle 0$. Similarly, the decrease in voltage during intervals 3 and 5 because of the reinjection bridge commutations were found in the same way, giving values of zero and $V_1 N_R\sqrt{2-\sqrt{3}} \quad \angle \tan^{-1}(\sqrt{3}-2)$, respectively.

The average decrease in dc voltage (ΔV_{DC}) over the main bridge switching interval is

$$\Delta V_{DC} = \frac{6}{\pi}\int_{\alpha}^{\alpha+\mu_M} \frac{(1 - N_R)}{2}\sqrt{2}V_1 \sin(\omega t)\, d\omega t + \frac{6}{\pi}\int_{\alpha+20^\circ}^{\alpha+\mu_{R2}+20^\circ} N_R\sqrt{2-\sqrt{3}}\ \sqrt{2}V_1 \sin(\omega t - 15^\circ)\, d\omega t \tag{2-6}$$

By assigning $\mu=\mu_M=\mu_{R2}$ it is assumed that optimally minimum harmonic content of the ac current is obtained, therefore equation (2-6) becomes

$$\Delta V_{DC} = \frac{6}{\pi}\int_{\alpha}^{\alpha+\mu} \frac{(1 - N_R)}{2}\sqrt{2}V_1 \sin(\omega t)\, d\omega t + \frac{6}{\pi}\int_{\alpha}^{\alpha+\mu} N_R\sqrt{2-\sqrt{3}}\ \sqrt{2}V_1 \cos(5^\circ)\sin(\omega t)\, d\omega t + \frac{6}{\pi}\int_{\alpha}^{\alpha+\mu} N_R\sqrt{2-\sqrt{3}}\ \sqrt{2}V_1 \sin(5^\circ)\cos(\omega t)\, d\omega t \tag{2-7}$$

By virtue of the nominal firing angle of the NC-SVC being near 90° the latter term in equation (2-7) is negligible. With reference to equation (2-2) the decrease in dc voltage is

$$\Delta V_{DC} \approx \frac{6}{\pi}\left((1-N_R) + 2N_R\sqrt{2-\sqrt{3}}\ \cos(5^\circ)\right)(1-N_R)X_{MC}I_{DC} = K_e X_{MC} I_{DC} \tag{2-8}$$

Comparing the effective commutating resistance for a conventional 12-pulse convertor ($\frac{6}{\pi}X_{MC}$) to equation (2-8) shows that a convertor containing the reinjection scheme has less effective commutating resistance by a factor of 0.351.

2.2.2 Operating mode transition

When the main and reinjection bridge commutation intervals are equal the transition from single to multiple commutation mode occurs when all commutation intervals equal 10°. At this operating point the firing angle is α_{mt}, as shown in figure 2-7. From equation (2-3),

$$\alpha_{mt} = \tan^{-1} \frac{\cos(10°) - 1 + \dfrac{X_{MC}(1-N_R)\dfrac{12}{\pi}}{R + k_e X_{MC}}}{\sin(10°)} \qquad \textbf{(2-9)}$$

Ideally, R = 0 and the commutation overlap begins when α_{mt} equals 84.9°. As the resistance is increased this angle is reduced. In what is considered an extreme case, where $R = X_{MC}$, i.e. the compensator is very inefficient, the firing angle is 77.2°. Compare these values to the equivalent 12-pulse NC-SVC case, i.e. 75° and 67°, and the 36-pulse NC-SVC has a firing angle range that is a factor of three smaller than the 12-pulse scheme. The magnitude of the fundamental current at the secondary of the main transformer ($I_{RMS(F)}$) is effectively proportional to I_{DC} (i.e. $I_{RMS(F)}=0.795I_{DC}$), hence I_{mt} equals $2x0.795I_{DC}$ when the firing angle is α_{mt}. Using equation (2-1) the corresponding values of I_{mt} for the range of firing angles and resistances describe above, show a 0.5 % variation, i.e. I_{mt} is effectively independent of resistance. The maximum compensator current is the short circuit current (I_{sc}), which is given by

$$I_{sc} = \frac{V_1}{\sqrt{3}(X_T + \tfrac{1}{2}X_S)} \qquad \textbf{(2-10)}$$

(Stigant *et al.*, 1973) where X_T and X_S are the primary side and secondary side reactances associated with the main transformer and ac supply. Given that R = 0, the value of I_{mt} with respect to the short circuit current is

$$\frac{I_{mt}}{I_{sc}} = 0.795\left(\frac{\frac{6\sqrt{2}}{\pi}\cos(\alpha_{mt})}{k_e X_{MC}}\right)2\sqrt{3}\left(X_T + \tfrac{1}{2}X_S\right) \qquad \textbf{(2-11)}$$

It is shown in chapter 3 that X_T must be much larger than X_S in order that the main and reinjection bridges commutation intervals are equal, i.e. $X_{MC} \approx X_T$, and $I_{mt}/I_{sc} \approx 0.987$. I_{sc} is typically 5 to 10 times the rated current of the convertor, therefore the NC-SVC has an inherent temporary overload capability without entering the multiple commutation mode, assuming that the components are rated accordingly.

2.3 A Comparison of component ratings

In this section the rating criteria for the components in the proposed compensator are defined, providing the basis for its design in later chapters. Moreover, ratings for the 12-pulse thyristor controlled reactor (TCR) (Miller, 1982) and 12-pulse naturally commutated SVC are also specified for the purpose of comparison. Note that these three topologies do not include VAr capacitors or ac filters.

Each of the three topologies use the same 3-phase transformer configuration with a secondary voltage of V_1. The reactive power rating, in terms of the ratings at the transformer secondary, is

$$Q = 6\left(\frac{V_1}{\sqrt{3}}\right) I_{RMS(F)} \qquad \textbf{(2-12)}$$

where $I_{RMS(F)}$ is the rated fundamental phase current. In the equations that follow all current, voltage, VA, inductance and capacitance ratings are normalised with reference to $I_{RMS(F)}$, V_1, Q, $(V_1^2/\omega Q)$ and $(Q/\omega V_1^2)$ respectively. The main results from this comparison are summarised in table 2-2. From this table it is evident that the cost of the reinjection scheme is small compared to the main convertor. The equivalent VAr rating of the blocking capacitors is approximately two orders of magnitude smaller than that of the dc reactor, the VAr rating of the reinjection transformer is approximately an order of magnitude smaller than the main transformer and the equivalent total VA rating of the thyristors in the reinjection bridge is approximately an order of magnitude smaller than the main convertor. In overview, assuming these ratings indicate the relative capital cost of the components, the cost of the reinjection scheme is approximately an order of magnitude smaller than the main convertor. Moreover, the naturally commutated configurations have $1/6^{th}$ the number of reactors than the TCR, but have approximately double the thyristor current rating, resulting in similar component requirements.

2.3.1 Main transformer

The VA rating of the 3-phase transformer (S), in terms of the ratings at the transformer secondary, is expressed as

$$S = 6\left(\frac{V_1}{\sqrt{3}}\right) I_{RMS} = \left(\frac{I_{RMS}}{I_{RMS(F)}}\right) Q \qquad \textbf{(2-13)}$$

where I_{RMS} is rated RMS phase current. In the case of the TCR, at rated power, the phase currents are sinusoidal (i.e. $I_{RMS} = I_{RMS(F)}$) and therefore the normalised VA rating is 1. For the 12-pulse naturally commutated SVC the theoretical values of I_{RMS} and $I_{RMS(F)}$ are

$0.817I_{DC}$ and $0.780I_{DC}$ respectively, assuming no thyristor commutations, giving a normalised VA rating of 1.05. The 36-pulse naturally commutated SVC with theoretical values for I_{RMS} and $I_{RMS(F)}$ of $0.927I_{DC}$ and $0.795I_{DC}$ respectively, give a normalised rating 1.17.

2.3.2 Main thyristors

In all three cases the peak reverse voltage experienced by the main thyristors is $\sqrt{2}V_1$. Moreover, all the thyristors are switched at this maximum voltage and the rate of change of voltage stresses for these thyristors are equal.

The current rating in the thyristors depends on the current waveshape. This is because the power loss is dominated by semiconductor conduction losses as well as junction losses that are inherent in the thyristor [IEEE 1158, 1991]. The RMS and average current values are both needed to define the current rating. Since I_{RMS} is the rated RMS phase current at the transformer secondary and the thyristor/reactor units of the TCR are connected in a delta configuration the thyristor RMS current is $1/(\sqrt{2}\sqrt{3})$. Similarly the normalised average thyristor current is $\sqrt{2}/(\sqrt{3}\pi)$. Considering the ac/dc conversion alternatives, the RMS current in the main bridge thyristors is $I_{RMS}/\sqrt{2}$ and the average current $I_{DC}/3$, which after substitution and normalisation give the following RMS and average values of thyristor current

12-pulse configuration: $\dfrac{0.817}{0.780\sqrt{2}}$ and $\dfrac{1}{0.780 \times 3}$

36-pulse configuration: $\dfrac{0.927}{0.795\sqrt{2}}$ and $\dfrac{1}{0.795 \times 3}$

The maximum rate of change of current in each thyristor is also an important factor in the thyristor specification. For the TCR the maximum current is sinusoidal, therefore the rate of change is equal to the peak of the sine, i.e. $\sqrt{2}\times(1/\sqrt{3})$. For the 12-pulse NC-SVC the rate of change is determined by the commutation interval. Since the firing angle is near 90°, the current changes linearly with a rate of $(\sqrt{3}/\sqrt{2})I_{sc}$, where I_{sc} is the short circuit current at the transformer secondary winding. The reinjection of 6^{th} harmonic current into the main convertor of the proposed scheme results in the maximum rate of change of current to occur

during the switching of the reinjection bridge and has a magnitude of $\frac{N_R}{1 - N_R}(\sqrt{3}/\sqrt{2})I_{sc}$.

With an I_{sc} five times the rated current, the normalised rate of change of current rating is $(\sqrt{3}/\sqrt{2})\times 5$ and $\frac{0.658}{0.342}(\sqrt{3}/\sqrt{2})\times 5$ for the 12 and 36-pulse compensators, respectively.

2.3.3 Reactors

In the case of the TCR, reactor inductance is determined by the reactive power rating. Being a delta configuration, the inductance is

$$L = \left(\frac{V_1^2}{\omega Q}\right) 6 \qquad \textbf{(2-14)}$$

and the RMS current rating is $I_{RMS}/\sqrt{3}$.

The dc reactor in the naturally commutated SVC must be rated for the dc current, which is equal to $I_{RMS(F)}/0.780$ and $I_{RMS(F)}/0.795$ for the 12-pulse and 36-pulse schemes respectively. The dc reactor inductance in both the 12 and 36-pulse NC-SVC influence the harmonic distribution of the dc and ac currents, and the dynamic characteristics of the compensator. Whichever gives the largest inductance value determines the inductance required.

2.3.3.1 Inductance value from dc side harmonic levels

For the 36-pulse NC-SVC, as described in section 2.1.1, the 36^{th} harmonic is the lowest significant harmonic on the dc voltage. It can be shown, neglecting commutation and assuming infinite blocking capacitors, that at 90° firing angle the ratio of the peak to peak current ripple magnitude to rated dc current ($I_{RP}^{\%}$) is

$$I_{RP}^{\%} = \frac{\frac{2\sqrt{2}\ V_1 \mathrm{Cos}(15°)}{\omega L_{DC}}\left(1 - \mathrm{Cos}\left(\frac{\pi}{p}\right)\right)}{I_{DC}} \times 100\% \qquad \textbf{(2-15)}$$

where p is the pulse number. Since $I_{RMS(F)} = 0.780 I_{DC}$, p = 12 and using equation (2-12), the dc reactor inductance for a 12-pulse naturally commutated SVC is

$$L_{DC|p=12} = \frac{400\sqrt{6}\ \mathrm{Cos}(15°)\ V_1^2}{\omega I_{RP}^{\%}\ 0.780\ Q}\left(1 - \mathrm{Cos}\left(\frac{\pi}{12}\right)\right) \qquad \textbf{(2-16)}$$

For the 36-pulse case, since $I_{RMS(F)} = 0.795I_{DC}$, p = 36 and using equation (2-12), then equation (2-15) becomes

$$L_{DC|p=36} = \frac{400\sqrt{6}\ \mathrm{Cos}(15°)\ V_1^2}{\omega I_{RP}^{\%}\ 0.795\ Q}\left(1 - \mathrm{Cos}\left(\frac{\pi}{36}\right)\right) \qquad \textbf{(2-17)}$$

Equations (2-16) and (2-17) show that the inductance value is inversely proportional to $I_{RP\%}$, therefore there is a compromise between increasing the inductance to reduce the harmonics, and cost. A dc current ripple level of 10% of the rated dc current (i.e. $I_{RP}^{\%} = 10\%$) is considered acceptable since this results in a realistic dc reactor inductance. The normalised inductance values for the 12 and 36-pulse cases are 3.4 and 0.38, respectively. Comparison of these values with section 2.3.3.2 show that the latter values are larger and are used in table 2-2.

2.3.3.2 Inductance value from compensator dynamics

Assuming the controller of the NC-SVC uses a phase lock loop to synchronise the thyristor firing pulses to the ac voltage, which is discussed in chapters 3 and 4, a disturbance in the ac supply can cause a phase shift in the ac voltage and effectively change the firing angle. The thyristors switch to an ac phase that has a large voltage at that time, causing the dc voltage to suddenly increase. Being naturally commutated, the thyristors are unable to switch to another phase of lower voltage. Thyristor firings must be delayed to let the dc voltage naturally decrease according to the sinusoidal waveform. While the dc voltage is abnormally high the dc current will increase according to the dc reactor value, independent of the pulse number of the compensator. There is a compromise value for the reactor which will limit abnormal current change while maintaining the dynamic performance needed for the compensator. For an effective firing angle change of $\Delta\alpha$ the change in dc current (ΔI_{DC}) is approximately

$$\begin{aligned}\Delta I_{DC} &= \frac{1}{\omega L_{DC}}\int_0^{\Delta\alpha} \sqrt{2}\sqrt{2+\sqrt{3}}\ V_1 \sin\omega t\ \ d\omega t \\ &= \frac{\sqrt{2}\sqrt{2+\sqrt{3}}\ V_1}{\omega L_{DC}}(1 - \cos(\Delta\alpha))\end{aligned} \qquad \textbf{(2-18)}$$

With reference to equation (2-12) and $I_{DC} = 0.795I_{RMS(F)}$, the percentage change in current

with respect to the rated level ($\Delta I_{DC}^{\%}$) is

$$\Delta I_{DC}^{\%} = \frac{\Delta I_{DC}}{I_{DC}} \times 100 = \frac{6\sqrt{2}\sqrt{2+\sqrt{3}}}{0.795\sqrt{3}\ \omega L_{DC}}\left(\frac{V_1^2}{Q}\right)\left(1 - \cos(\Delta\alpha)\right) \times 100 \qquad \textbf{(2-19)}$$

An ac supply voltage phase shift of 20° caused by an ac disturbance, with a corresponding percentage change in current of 15% is considered a worst case situation. The inductance for the naturally commutated compensator is

$$L_{DC} = \frac{600\sqrt{2}\sqrt{2+\sqrt{3}}}{0.795\sqrt{3} \times 15}\left(\frac{V_1^2}{\omega Q}\right)\left(1 - \cos(20°)\right) \qquad \textbf{(2-20)}$$

The normalised value is 5.0. This is larger than the values obtained in section 2.3.3.1 and is used in table 2-2.

2.3.4 Reinjection transformers

As shown in figure 2-2, the voltage ripple in V_{B1} and V_{B2} is applied to each reinjection transformer and is at a maximum at 90° firing angle. This voltage ripple is characterised by $-\sqrt{2}V_1\sin(\omega t)$ for ωt in the range -30° to +30° and the RMS voltage on the primary side of the reinjection transformer is

$$V_{RMS} = V_1\sqrt{1 - \frac{3}{\pi}\sin(60°)} \qquad \textbf{(2-21)}$$

The RMS value of the current in the reinjection bridge side of the transformer is $(\sqrt{2}I_{DC})/\sqrt{3}$. Since $I_{RMS(F)} = 0.795I_{DC}$ and using equation (2-12), the VA rating is

$$\begin{aligned} S &= \left(\frac{0.658}{0.795}\sqrt{\frac{2}{3}}\ I_{RMS(F)}\right)\left(V_1\sqrt{1 - \frac{3}{\pi}\sin(60°)}\right) \\ &= \left(\frac{0.658}{0.795}\ \frac{\sqrt{2}}{6}\right)\left(\sqrt{1 - \frac{3}{\pi}\sin(60°)}\right)Q \end{aligned} \qquad \textbf{(2-22)}$$

By virtue of its operating frequency the size of this transformer is significantly smaller than

its 50 Hz equivalent. Chryssis (1989) states that size is inversely proportional to the square root of operating frequency, therefore the size is reduced by a factor of 0.4.

2.3.5 Reinjection thyristors

With reference to table 2-1, which describes the construction of V_{B1} and V_{B2} from the phase voltages, and assuming large blocking capacitors, the commutating voltage of the reinjection bridge is

$$V_{RJ} = N_R(V_{B1} - V_{B2}) = N_R V_1 \sqrt{2 - \sqrt{3}} \angle -15° \qquad \textbf{(2-23)}$$

Therefore, the normalised ideal peak reverse voltage applied to the reinjection bridge (MAX(V_{RJ})) is $0.658\sqrt{4 - 2\sqrt{3}}$. In the same way as described for the main thryistors, the switching occurs near the voltage maximum and the dv/dt is at its maximum. Moreover, the current ratings for the thyristors must be specified in terms of average and RMS currents. The RMS thyristor current is $I_{DC}/\sqrt{3}$, which, in terms of $I_{RMS(F)}$, becomes $1/(0.795\ \sqrt{3})$ after being normalised. Similarly the average thyristor current $I_{DC}/3$ is normalised to 1/(0.795 x 3). The reinjection bridge must commutate in the same interval as the main bridge to fully cancel the ac current harmonics, therefore the di/dt of the reinjection bridge thyristors is $1/N_R$ times the main bridge thyristors. Continuing with the assumption that the short circuit current is 5 times the rated current, the normalised rate of change of current is $\frac{1}{0.324}(\sqrt{3}/\sqrt{2})\times 5$.

2.3.6 Reinjection capacitors

The blocking capacitors have two voltage components; the average of the main bridge dc voltage and a 6th harmonic voltage that is generated by the flow of reinjection current through the capacitor. In steady state the former is ideally zero because the dc impedance is purely inductive. The latter, ideally, generates a peak voltage across the capacitor (V_c) of

$$V_C = \frac{1}{\omega C}\int_0^{\frac{\pi}{18}} N_R I_{DC}\, d\omega t = \frac{\pi N_R I_{DC}}{18\omega C} \qquad \textbf{(2-24)}$$

The polarity of the 6th harmonic voltage across capacitors C_1 and C_2 means that their sum appears at the secondary of the reinjection transformer. This voltage increases the ideal peak reverse voltage rating of the reinjection bridge, discussed in section 2.3.5, by $2N_R V_c$. The

percentage increase in the reinjection bridge voltage ($\Delta V_{RJ}^{\%}$) is

$$\Delta V_{RJ}^{\%} = \frac{2V_C N_R}{MAX(V_{RJ})} = 2\left(\frac{\pi N_R^2 I_{DC}}{18\omega C}\right)\left(\frac{1}{N_R\sqrt{4 - 2\sqrt{3}}\, V_1}\right) \times 100\% \qquad \textbf{(2-25)}$$

Since $I_{RMS(F)} = 0.795 I_{DC}$ and using equation (2-12), equation (2-25) can be rewritten in the form

$$C = \left(\frac{Q}{\omega V_1^2}\right)\frac{11.4}{\Delta V_{RJ}^{\%}} \qquad \textbf{(2-26)}$$

Equation (2-26) shows that there is an inverse relationship between C and $V_{RJ}^{\%}$, therefore there is a compromise between reducing capacitance and cost, at the expense of increasing the reinjection bridge rating and cost. A 10% increase of reinjection bridge rating is considered acceptable and is used in the comparison of table 2-2 since it results in a realistic capacitance.

In steady state, equation (2-24) specifies the peak voltage across the capacitor, but during a dynamic event the average dc voltage from the main bridge will be nonzero. The variation of average dc voltage during a dynamic event is dependent on the controller algorithm. The worst case transition is assumed to be when the dc current must undergo a step increase. The average dc voltage will change from the zero to maximum voltage to force the reactor current to increase. The commutation interval increases with current, reducing the average dc voltage. Note that the polarity of these dc voltages are such that its presence is cancelled at the reinjection transformer secondaries and they do not affect the operation of the reinjection scheme.

The blocking capacitor is in series with the reinjection transformer and any charging currents to increase the capacitor voltage must flow through the magnetising inductance of the transformer(L_m), forming an LC resonant circuit. Assuming a linear magnetising characteristic, the time constant of the dc impedance is orders of magnitude smaller than that of the L_mC resonance. With respect to the L_mC oscillation, the dc voltage transition is equivalent to an impulse ($V_{DC}^{*}\delta(t)$), where its magnitude, V_{DC}^{*}, is equal to the integral of the dc voltage during the transition. Assuming the dc current changes from zero to I_{DC},

$$V_{DC}^{*} = \int_0^{\infty} V_{DC}\, dt = L_{DC}\int_0^{I_{DC}} dI_{DC} = L_{DC}I_{DC} \qquad \textbf{(2-27)}$$

Half of this dc voltage is applied to each resonant circuit, therefore, assuming that there is no resistance in the L_mC oscillation, the average dc component of the capacitor voltage reaches

	12-pulse TCR	12-pulse NC-SVC	36-pulse NC-SVC
3 phase transformer:			
-VA rating	1	1.05	1.17
Main thyristors:			
-number	12	12	12
-Peak reverse voltage	1.41	1.41	1.41
-RMS current	0.408	0.741	0.825
-Average current	0.260	0.427	0.419
Reactors:			
-number	6	1	1
-Inductance value	6	5.0	5.0
-Current rating (RMS)	0.577	1.28	1.26
Reinjection thyristors:			
-number			5
-Peak reverse voltage	NOT	NOT	0.482
-RMS current	APPLICABLE	APPLICABLE	0.726
-Average current			0.419
Reinj. transformers:			
-number	NOT	NOT	2
-VA rating	APPLICABLE	APPLICABLE	0.071
Reinj. capacitors:			
-number			2
-capacitance value	NOT APPLICABLE	NOT APPLICABLE	1.14
-peak voltage			0.082

The normalising factors are: Current $I_{RMS(F)}$, Voltage V_1, Power Q,

Inductance $V_1^2/\omega Q$, Capacitance $Q/\omega V_1^2$

Table 2-2: Normalised component rating summary.

a maximum of

$$V_C = \frac{L_{DC}I_{DC}}{2}\left(\frac{1}{\sqrt{L_mC}}\right) \quad \textbf{(2-28)}$$

Using equations (2-24) and (2-12), the total voltage rating of the capacitor with respect to V_1 is

$$\frac{V_C}{V_1} = \left(\frac{L_{DC}}{2\sqrt{L_mC}} + \frac{\pi N_R}{18\omega C}\right)\frac{Q\sqrt{3}}{6V_1^2\ 0.795} \quad \textbf{(2-29)}$$

From the reinjection transformer ratings in section 2.3.4, L_m can be specified in terms of fundamental frequency magnetising current with respect to the rated current ($I_m^{\%}$), where $L_m=(V_1^2/Q)(213/\omega I_m^{\%})$. With $I_m^{\%}=0.5\%$ and using values from table 2-2, the maximum capacitor voltage is 8.2% of V_1. The dynamic term of equation (2-29) can become insignificant by making $I_m^{\%}$ sufficiently small, but there is a compromise between reducing capacitor voltage and increasing transformer size needed to achieve the lower $I_m^{\%}$ value.

2.4 Conclusion

The 36-pulse naturally commutated SVC utilises a naturally commutated ac/dc convertor that is dedicated to the control of reactive power. The convertor consists of a conventional 12-pulse configuration and a reinjection scheme that modifies the 12-pulse ac current and dc voltage waveforms to resemble 36-pulse. The pulse multiplication is approximate, but the residual levels of 12-pulse related harmonics are significantly smaller than the characteristic. Commutation within the convertor is the main mechanism that limits the compensator current magnitude as the firing angle is decreased from 90°. In steady state there is a linear relationship between current and firing angle over 98.3 % of the possible current range, i.e. zero to short circuit current. The firing angle range of this linear region is ideally approximately 5°, but this increases to 15° when the resistance equals the commutating reactance, i.e. in an inefficient scheme.

From the component ratings, it is estimated that the reinjection scheme has a cost that is an order of magnitude smaller than the main convertor. The comparison of component ratings between the 36-pulse NC-SVC and the two alternatives (12-pulse thyristor controlled reactor, 12-pulse NC-SVC) showed that there is not a significant difference in component rating.

Chapter 3

Hardware modelling

As discussed in chapter 1, the proposed 36-pulse naturally commutated SVC is intended to have a power rating in the MVAr range, suitable for high voltage applications. It is outside the scope of this research to implement an actual unit for the purposes of confirming the operating predictions described in chapter 2.

Hardware modelling, described in this chapter, is one of two modelling techniques used in this thesis to illustrate the operation of the actual unit, thus confirming the theory. It relies on the component characteristics scaling linearly as the compensator rating is decreased to a level suitable for the laboratory. The second modelling technique uses software and is described in chapters 4 and 5.

Although the 2.6 kVAr hardware model described in this chapter has excessive damping, making it unsuitable for dynamic studies, it is still useful when considering steady state operation. In particular, measured waveforms and operating characteristics from the model are compared to the theoretical characteristics discussed in chapter 2. Moreover, the influence of component values on the ac current harmonic content and steady state operating characteristic are considered. Finally, the influence of the component values on the reinjection bridge commutation is analysed and verified with measured results.

3.1 Model description

Scaling down of the power components in the compensator presents several problems, the main one being the presence of a significant magnetising current, and therefore harmonic content, in the model transformers (Stigant *et al.*, 1973). The harmonic levels of the

compensator current are an important part of its viability and the masking of this information by magnetising current harmonics must be avoided. The problem is alleviated by operating the model at 80% of the "name plate" voltage, to reduce the level of saturation in the transformer, and with it the magnetising current harmonics (Bean *et al.*, 1959) (harmonic levels are listed in Appendix A). In addition, compared to typical power system transformers, the main transformer has a smaller percentage reactance and is corrected by adding reactance in series on the primary side. Furthermore, all the components in the compensator, as well as the synchronous generator, which provides the ac voltage source for the model, have larger percentage resistance than their high power equivalents (Stigant *et al.*, 1973; Weedy, 1979) (values listed in Appendix A) increasing the damping of the circuit. The values used for the dc reactor (L_{DC} = 2.8 mH) and blocking capacitors (C = 1500 μF) are derived from the criteria discussed in chapter 2. For the dc reactor value, it is assumed that there are no events in the ac circuit that cause ac disturbances and the steady state specification is applicable.

As mentioned in chapter 2, the correct combination of main and reinjection bridge thyristors must be fired at regular intervals in synchronism with the ac voltage, i.e. 36 times per ac cycle. There are significant advantages in using digital based firing controllers (Arrillaga *et al.*, 1970; Pontes Parente *et al.*, 1985) and the continued development of digital computers provides increasing scope for control possibilities (Tso *et al.*, 1981; Mirbod *et al.*, 1986; Haddock *et al.*, 1993). A recent addition to the field of controller implementation is the digital signal processor (DSP) (Texas Instruments, 1990) and is used in the hardware model. This system uses a TMS 320C30 processor, which is characterised by a 32 bit data bus, 60 ns instruction period and floating point arithmetic hardware (Texas Instruments, 1992). As well as precise timing for the firing of the thyristors, this processor permits the implementation of complex control algorithms. For example, the DSP could be used to monitor the ac current harmonic content for use as a control feedback signal. The control block would modify the firing angle in such a way as to minimise the harmonics (Farret *et al.*, 1990).

Essentially, the controller consists of two phase lock loops (PLL) (Ainsworth, 1968), as shown in figure 3-1, which receive the firing angle command and generate the appropriate timing signals for the thyristor drivers. PLL #1 locks onto the ac voltage frequency (using the zero crossing information), thus generating a filtered timing representation of that voltage within the DSP. PLL #2 automatically operates at the same frequency as PLL #1, but incorporates a phase delay specified by the firing angle command, frequency multiplication to provide 36 pulses per ac cycle, and timing correction to account for variable processing delays in the DSP. Variable processing delays are correctable by forcing all program branches to have the same execution time and ensuring that multiple interrupt service routines do not clash, in which case PLL #2 becomes a controlled oscillator. The implemented program has two interrupts, one for PLL#1 and another for PLL#2, and their variable phase means that the

potential for interrupt clashes exists. Maintaining a constant phase between interrupt routines (and avoiding clashes) requires the zero crossing detection to be replaced with waveshape measurement of the ac voltage for use in the PLL (Manitoba HVDC, 1988).

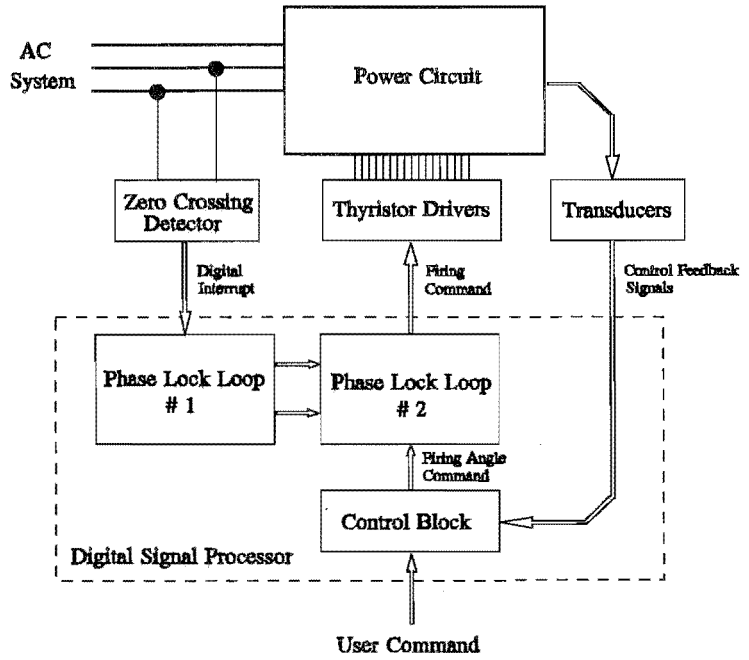

Figure 3-1: Controller for the naturally commutated SVC.

3.2 Experimental verification of waveforms

The predicted operation of the ac/dc convertor, described in chapter 2, is confirmed in the following sections using measured waveforms from the hardware model. The comparison of the theoretical and experimental is simplified by maintaining the same format in the coming sections as in section 2.1. i.e. the voltage and current conversion processes are considered separately.

3.2.1 Measured voltage waveforms

The trends in the measured voltages, shown in figure 3-2, compare well with the theoretical waveforms in figure 2-2, supporting the predicted operation. The measured waveforms, however, contain the effects of both the main and reinjection bridge commutations. As an example, at approximately 3.1 ms in figure 3-2 there is a main bridge commutation. This voltage transition is observed in all the waveforms, occurring slower than shown in theory because of the snubbers across the switches (Williams, 1992). The commutation "step" is barely visible, but is evident in figure 3-2(b).

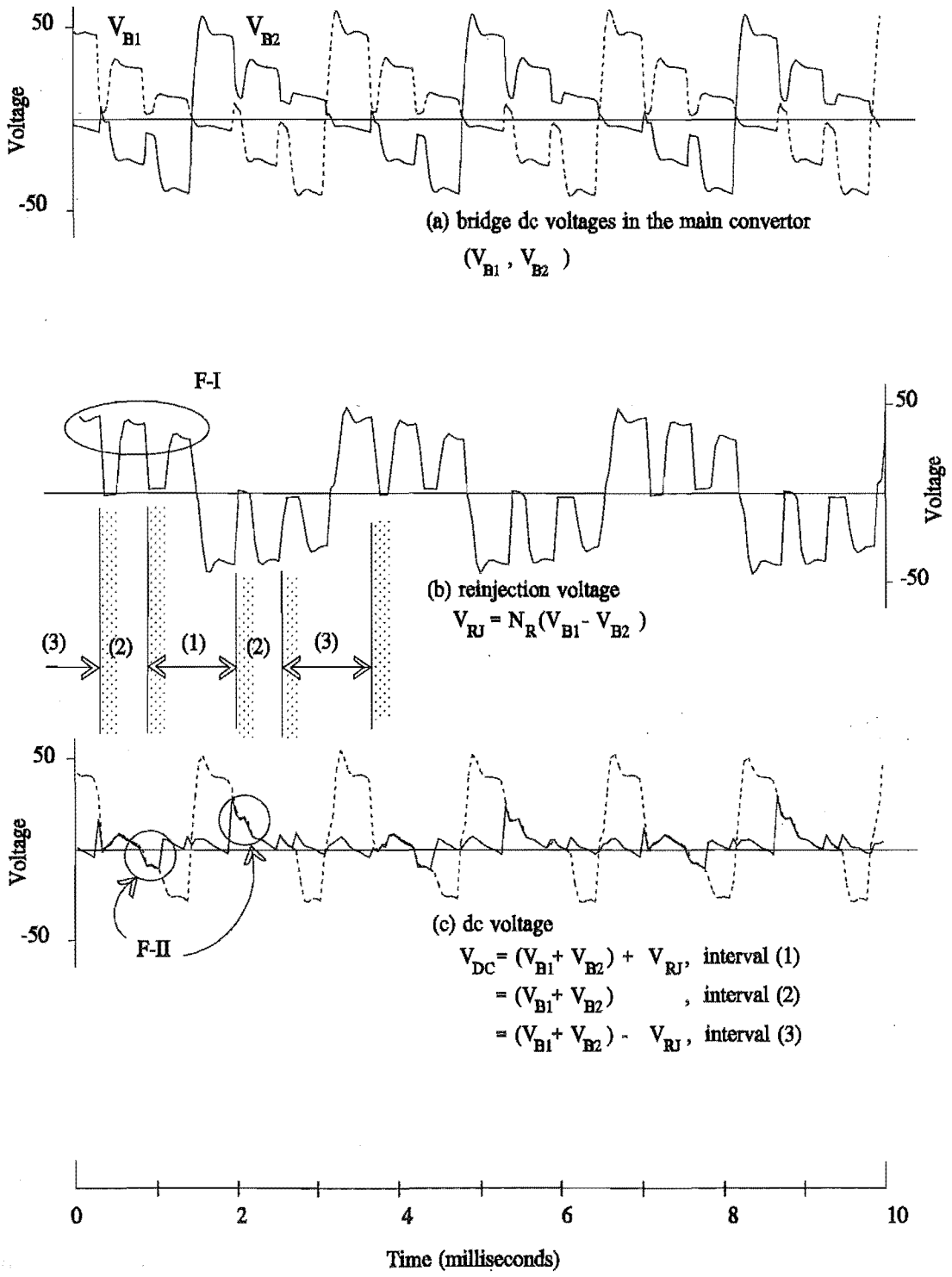

Figure 3-2: Experimental voltage waveforms

With reference to the reinjection bridge commutations, the secondary side output of the reinjection transformers is shorted, i.e. the reinjection voltage is zero, identified in figure 3-2(b) by shaded regions in intervals (1), (2) and (3). Comparing the commutations shows that the main bridge commutation interval is significantly shorter than the reinjection bridge and is a cause of asymmetry in the 36-pulse dc voltage. During the reinjection bridge commutations the dc voltages of each main bridge are forced to be equal (i.e. $V_{B1}=V_{B2}$) because of the relative orientation of the reinjection transformers. The presence of impedances between the commutating switches and the main bridges, however, maintain a small voltage difference, as shown in figure 3-2(a).

Ignoring the commutation "notches" in figure 3-2(b), the waveshape of the measured V_{RJ} differs from ideal because it includes the voltages generated across the blocking capacitor and resistances inherent in the circuit. As an example, consider one conduction interval of the main bridge, shown as feature F-I in figure 3-2(b). Ideally, the reinjection voltage is approximately constant because this portion of the waveform is formed from the apex of a fundamental frequency sinusoid. In the hardware model the voltages across the resistances and capacitors (shown in figure 3-11, where the voltage across the resistances is proportional to the reinjection current) subtract from the commutating voltage. This results in V_{RJ} being significantly larger in interval (3) than in interval (1). Modification of the reinjection voltage affects the reinjection bridge commutation and is the subject of section 3.5.2 and 3.5.5.

In any main convertor conduction interval there are two different reinjection bridge commutations. From the start of the first reinjection bridge commutation to the end of the second the 36-pulse dc voltage waveshape equals the 12-pulse dc voltage, as shown in figure 3-2(c) (where the dotted trace is the 12-pulse waveform).

According to table 2-1, the 12-pulse dc voltage waveshape is not modified by the reinjection bridge commutation, and both the 12 and 36-pulse voltages contain a single sinusoidal portion during this interval. Figure 3-2(c) shows, however, that this is not the case for the hardware model because the two main bridge voltages are not balanced. This unbalance results in the dc voltage (during the commutation) being decreased in one main bridge interval and increased in the next, shown as feature F-II in figure 3-2(c). Therefore, the main bridge imbalance propagates through the reinjection scheme and appears at the 36-pulse dc voltage at the 6^{th} harmonic.

3.2.2 Measured current waveforms

Measured currents from the hardware model when the dc current is 12.1 amps are shown in figure 3-3. In addition, the measured supply voltage (phase to neutral) is included in figure 3-3(d) to give an idea of total distortion and phase angle displacement of the

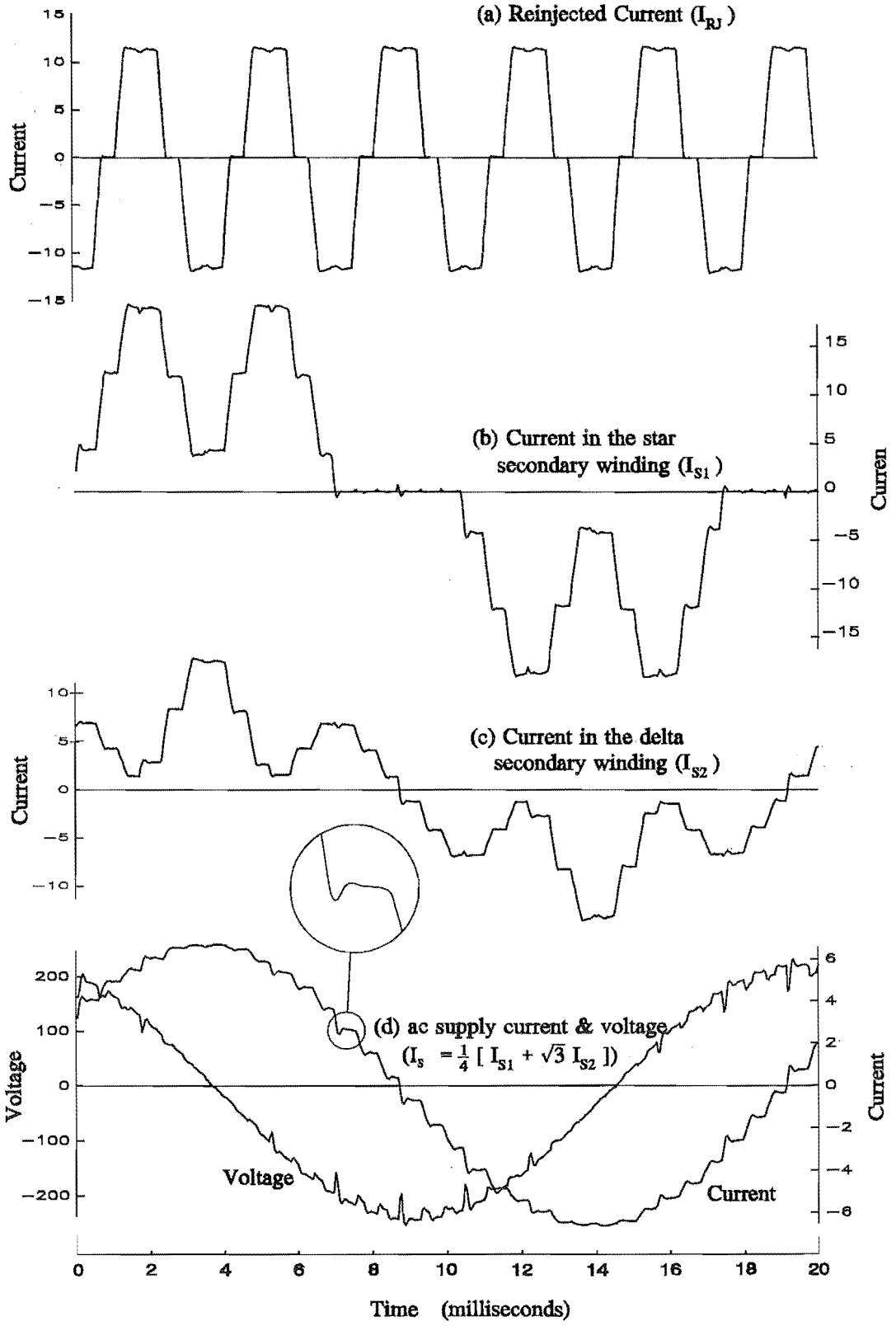

Figure 3-3: Experimental current and supply voltage Waveforms.

compensator current (approximately 90°).

The voltage waveforms described in section 3.2.1 are distorted because of impedances in series with the current flow. By virtue of the dc reactor acting as a dc current source, these series impedances have little effect on the current waveshapes. Therefore, the measured currents show better agreement with the theoretical equivalents (in figure 2-4) than their voltage counterparts, significantly improving the confidence in the predicted operation. The main difference between the ideal and experimental current waveforms is the slope of the current transitions due to the commutation process. Closer inspection of figure 3-3(d) shows that every third transition occurs in a shorter interval than the others, correlating with the main bridge having a shorter commutation than the reinjection bridge, as discussed in section 3.2.1.

With ideal 36-pulse operation, the harmonic orders below the 35^{th} are absent and the levels of the 35^{th} and 37^{th} are inversely proportional to the harmonic order. The 36-pulse related harmonics of the experimental waveform (figure 3-4) are slightly lower than the ideal as a result of the commutation overlaps. Moreover, the experimental spectrum contains small amounts of all harmonic orders. They are categorised into either typical convertor harmonics or harmonics specific to the reinjection scheme. The typical convertor harmonics include triplen and 6±1 harmonics, which are predominantly due to

(i) non-linearity of the magnetising characteristic of the main transformer (Bean *et al.*, 1959),

(ii) symmetries in the ac supply voltages, main transformer leakage reactances, control firings, etc. (Arrillaga, 1988)

Because of the reinjection scheme, small quantities of 12±1 and 24±1 harmonics are also present in the measured data and these are attributed to the

(iii) approximate nature of the pulse multiplication achieved by the reinjection scheme, as shown in figure 2-6,

(iv) 6^{th} harmonic voltage component of the blocking capacitor and resistances being added to the dc voltage as 12-pulse related harmonics,

(v) dc voltage waveform asymmetry caused by the presence of main and reinjection bridge commutations. This asymmetry is amplified when there is a difference in commutation intervals,

(vi) difference between the main and reinjection bridge commutation intervals.

In theory the 12n-1 and 12n+1 harmonics (where n=1,2,3,...) should be approximately equal in magnitude, as described in chapter 2. However, construction imperfections affecting the reinjection transformer turns ratio cause the 12n-1 harmonics to be different to the 12n+1 harmonics. Specifically, if N_R is reduced then the 12n-1 harmonics is larger than the 12n+1 harmonics and vice versa.

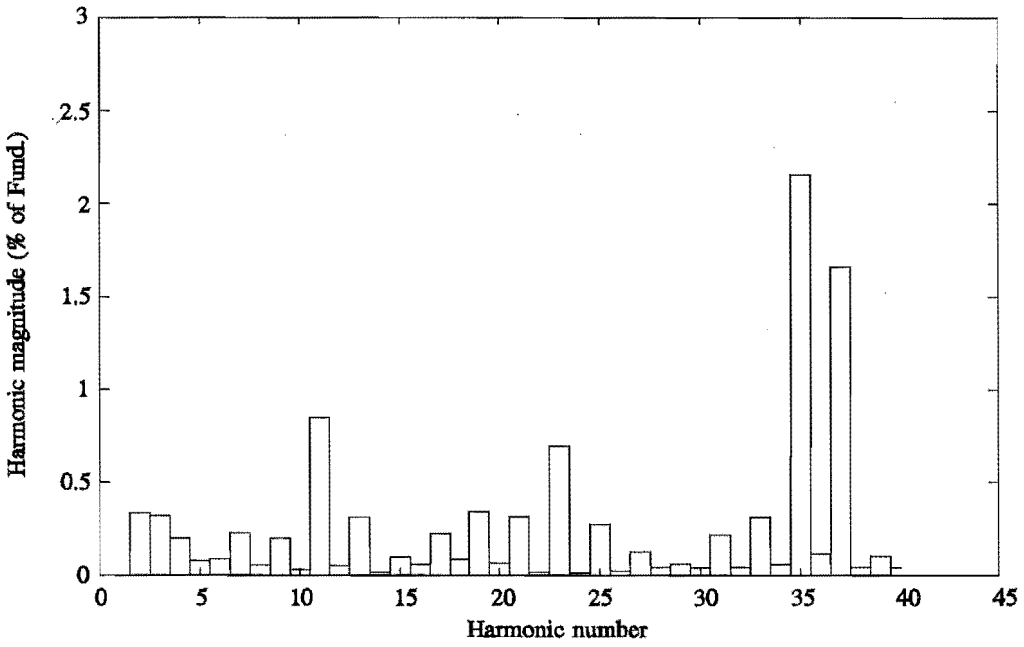

Figure 3-4: Harmonic content of the experimental supply current waveform.

3.3 Measured operating characteristic

The reactive power absorbed by the test system is adjustable from 0.26 kVAr (at $\alpha = 89°$) to the full 2.6 kVAr (at $\alpha = 80°$). This confirms the linear trend of the fundamental current with respect to firing angle, shown theoretically in figure 2-7. Below the 0.26 KVAR operating level the dc current periodically reaches zero, the conducting thyristors turn off and discontinuous mode is entered. Furthermore, with no commutations, some of the negative portions of the dc voltage waveform are removed and the rate of change of reactive current with firing angle decreases significantly.

Given that the short circuit current is 4.2 times the rated current (using the data in Appendix A), the slope of measured current (with respect to α) in the single commutation mode is an order of magnitude smaller than the theoretical current. This implies that the resistance inherent in the compensator plus the commutating resistance is an order of magnitude larger than predicted by theory. Although the hardware model has significant inherent resistance, the main difference in characteristic arises because the reinjection bridge commutation interval (average measurement is 125 μs) is significantly longer than the main bridge (measured at 45 μs). The derivation of commutating resistance, described in chapter 2, assumes that the commutation intervals are equal and specifies the effects of the reinjection bridge commutations in terms of the main bridge. When the reinjection bridge commutation is longer than the main bridge the average dc voltage is less than assumed for a given current.

In other words, the commutating resistance is larger than expected. Furthermore, a longer reinjection bridge commutation interval for a given current means that the maximum current in the single commutation mode (I_{mt}) is reduced compared to the short circuit current. The mechanisms that control the duration of the reinjection bridge commutation are discussed in detail in section 3.5.

Finally, the measured harmonic content of the ac current over the rated firing angle range is shown in figure 3-5. In this case the magnitude of the harmonics are specified relative to the full load fundamental component. The trend of the harmonic traces is similar to the theoretical, but as discussed earlier the firing angle range is significantly larger. In other words, the traces between 80° and 90° firing angle, shown in figure 3-5, are equivalent to those between 88.8° and 90° firing angle, in figure 2-7.

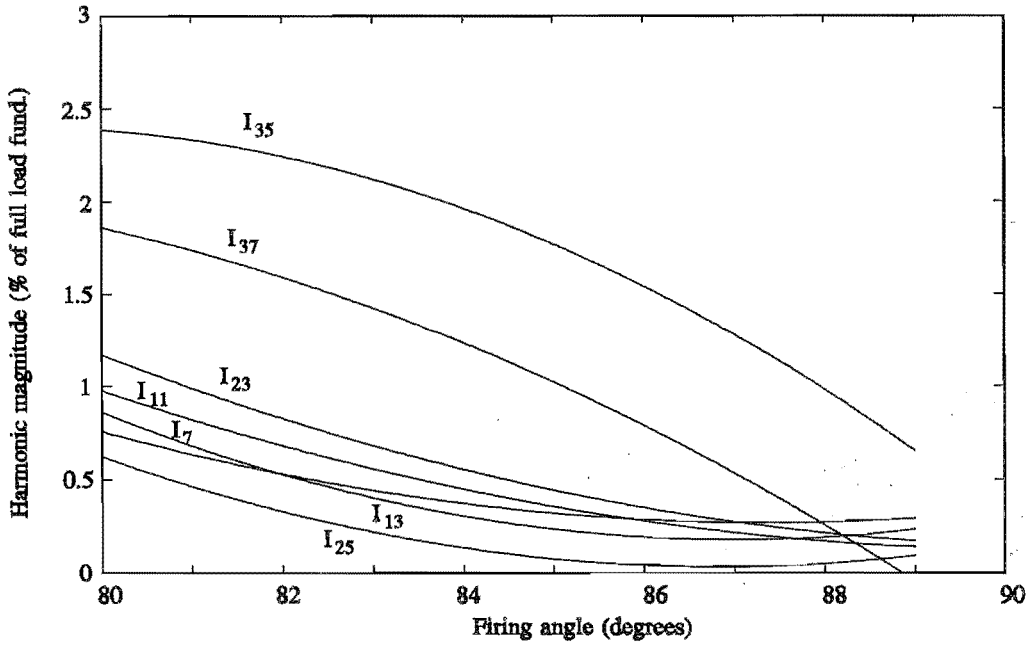

Figure 3-5: Experimental supply current harmonics over the operating range of the SVC.

A subtle difference in the trend of the 12±1 and 24±1 harmonic traces compared to theory is that the slope of these traces increase as the firing angle decreases, whereas the slope of the theoretical harmonics decrease in value, as shown in figure 2-7. This difference is attributed to the fact that the commutation intervals in the reinjection bridge (average measurement of 125μs) are not equal to the commutations occurring in main bridge (measured at 45μs), i.e. different by a factor of 2.8. As an example, consider the theoretical I_{11} and I_{13} harmonics, shown in figure 2-7 (and reproduced in figure 3-6). When the reinjection bridge commutation is three times that of the main bridge, the harmonics are increased to I_{11}^* and I_{13}^*, as shown in figure 3-6. The significance of the harmonic increase depends on the

compensators current level. Rated current for the hardware model is approximately $I_{sc}/4.2$ and at this level these harmonics are theoretically approximately 3 times larger than the case where the commutations are equal. In other words, the 11^{th} and 13^{th} harmonics are, theoretically, approximately 1.2% when the commutations are not equal. This compares well with the measured values, shown in figure 3-6, which are approximately 0.9%.

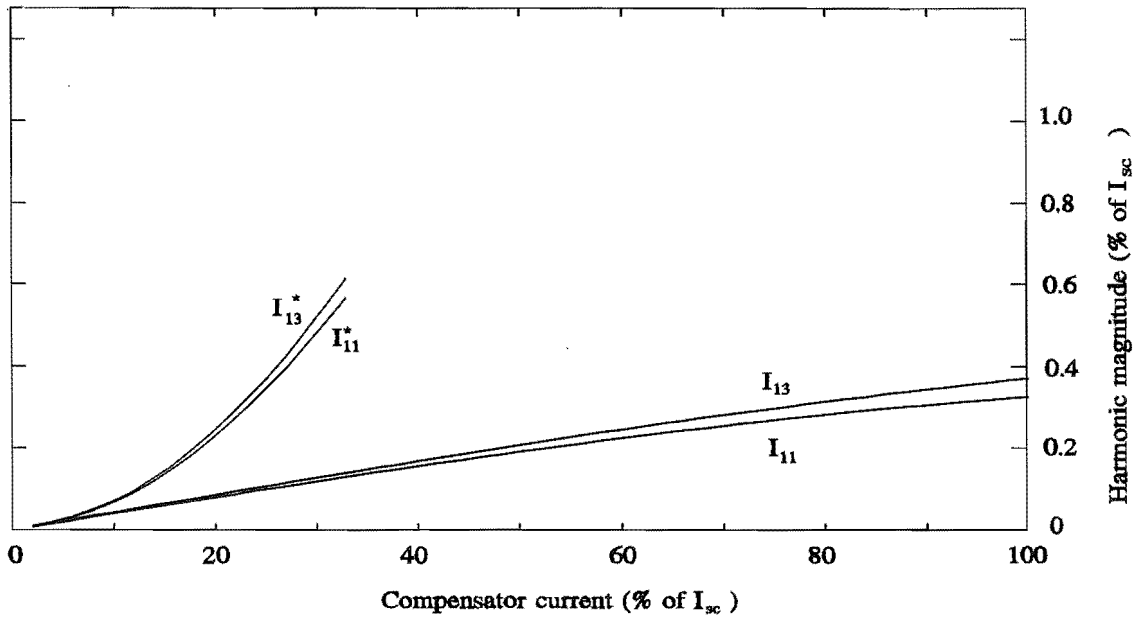

Figure 3-6: Theoretical steady state harmonic content (when $\mu_{R1}=\mu_{R2}=2\mu_M$)

3.4 Influence of component values on ac current harmonics

The viability of the compensator is dependent on the level of harmonic current produced, therefore it is important to find the influencing factors so these harmonics can be minimised. When the dc reactor and blocking capacitor are of finite size, they both modify the voltage and current waveshapes, and therefore modify the harmonic content of the compensator current. In chapter 2, these component ratings are specified in terms of their effect on the dc current and reinjection voltage, respectively. In this section the impact of these design criteria on the compensator harmonics is considered.

The variation of harmonic content as the dc reactor and blocking capacitor values are changed is shown in figure 3-7. The dc reactor size dominates the value of the dc impedance and therefore the relationship between dc voltage and dc current harmonics. As seen in the figure, when the dc reactor is larger than approximately 100 mH, the harmonic content is approximately constant (for a given capacitor value) i.e. the dc voltage harmonics have

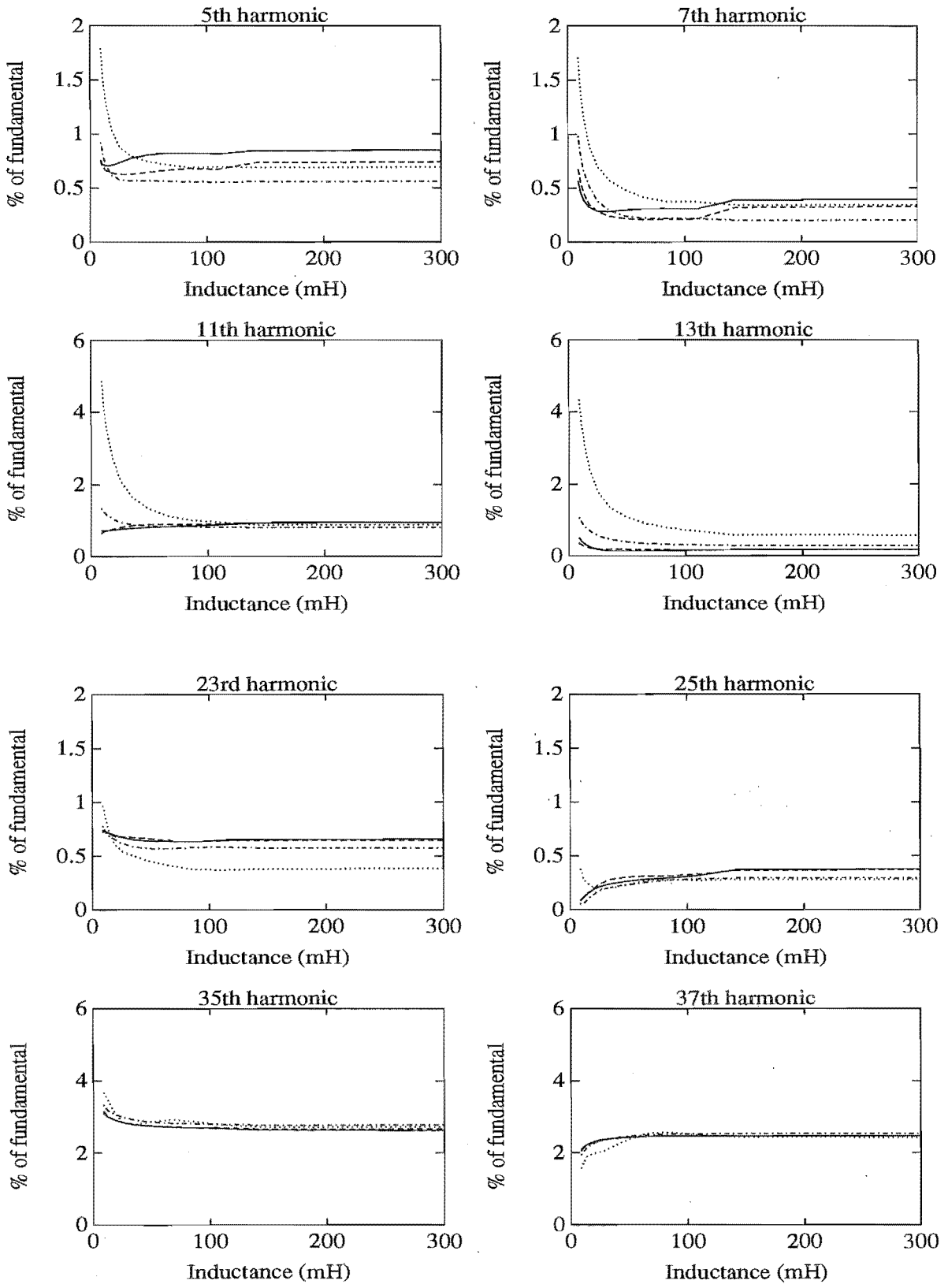

Figure 3-7: Compensator current harmonic content with different blocking capacitor and dc reactor values.

(_____ C=7300μF, _ _ _ _ _ C=1500μF, _._._._. C=200μF, ... C=50μF)

negligible effect on the dc current. Conversely, when the dc reactor is smaller than approximately 100 mH the dc voltage harmonics also appear on the dc current and are transferred to the ac current via the convertor. As specified in chapter 2, 100 mH is normalised to 13.4 and the normalised dc reactor values using ripple and dynamic specifications are 0.38 and 5.5, respectively. This shows that with either specification the dc voltage harmonics can not be neglected. Note that the dc side harmonics do not always increase the harmonic magnitudes of the current, it depends on their phase relative to the harmonics generated elsewhere. For the 25^{th} and 37^{th} harmonics their magnitudes decrease as the dc current harmonics increase.

The size of the capacitor has two observable effects on the harmonics. First, a small capacitor (where its 6^{th} harmonic voltage is significant) causes large dc voltage harmonics and when the dc reactor is small these harmonics appear in the ac current. Since the 6^{th} harmonic voltage across the blocking capacitors add to the reinjection voltage, and appears on the dc voltage as a 12^{th} harmonic, the 12±1 ac current harmonics are the worst effected. The second observable effect of capacitor size is the change in reinjection bridge commutation interval. Even with a smooth dc current (i.e. a large dc reactor) the difference between the main and reinjection bridge commutation intervals modify the ac current harmonics. As shown in figure 3-6, the change in harmonic content as the capacitor size is varied is minor (when the dc reactor is large) compared to the effect of the dc side harmonics (when the dc reactor is small).

Comparison of the C=7300 μF and C=1500 μF traces in figure 3-7 shows that there is negligible difference between the rated capacitor size in the hardware model and a pseudo-infinite capacitance. In other words, the rated capacitor has negligible effect on the compensator operation for the current level in the test. Reduction of the capacitance to 200 μF cause detectable changes in the traces, but a further reduction to 50μF is much more significant. This correlates the trend in figure 3-12, where the rate of change of commutation interval with respect to capacitance increases at smaller capacitance values.

3.5 Commutation intervals of the reinjection bridge

The reinjection bridge is commutated by the ac supply similar to the main bridge (Arrillaga, 1988), but the duration of these commutations are not automatically equal because their commutating impedances may differ. When the commutations are different the ac current harmonics are modified along with the relationship between firing angle and reactive current level, as discussed in section 3.3.

In the following sections an expression for the reinjection voltage is derived that is valid over a conduction interval of the main bridge. The two reinjection bridge commutations occurring

in that interval are different, but this expression describes both of them when V_{RJ} is forced to zero. These commutations are distinguished by referring to the first and second commutation that occurs in the main convertor conduction interval. The effect of the blocking capacitor and reactances associated with the transformer and ac supply are included in the theory and the result is compared with measurement. In the hardware model, the resistances inherent in the compensator are significant and its effect on the commutations is also measured.

3.5.1 Expression for the reinjection voltage

An equation describing the reinjection voltage is derived in two steps. The first is the definition of the ac voltages at the ac terminals of the main bridges, given that these voltages are modified by the flow of current through reactances inherent in the ac circuit. In this analysis the resistances are neglected. The second step relates to the voltages on the dc side of the main convertor and depends on the switching state of that convertor.

The ac supply and ac portion of the compensator are shown in figure 3-8. The ac supply is represented as ideal phase to neutral voltage sources (V_R,V_B,V_Y) in series with an inductive reactance. Phases of the supply are consistently labelled with subscripts R, Y and B throughout the circuit. Furthermore, in the following analysis a general subscript (i) is used where expressions are common to all phases.

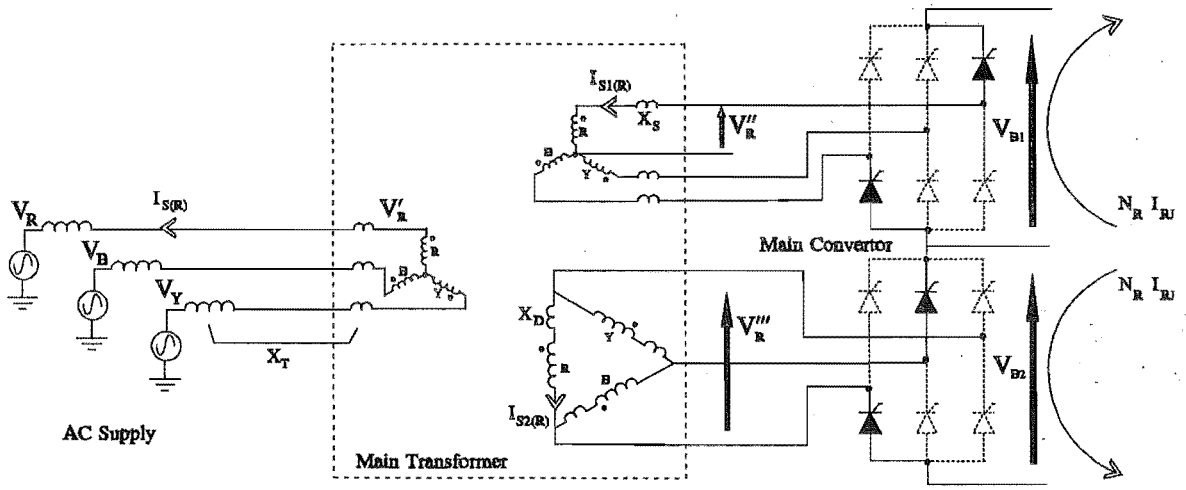

Figure 3-8: The ac supply and ac portion of the NC-SVC.

The main transformer is modelled as an ideal transformer with leakage inductance distributed between the primary and secondary windings. This allows the supply and primary leakage reactances to be lumped into a single component (X_T).

The phase to neutral voltage at the primary winding of the ideal transformer (V_i') is

$$V_i' = V_i + X_T \frac{dI_{S(i)}}{d\omega t} \tag{3-1}$$

where $I_{S(i)}$ is the ac supply current. Since $I_{S(i)} = (I_{S1(i)} + \sqrt{3}\, I_{S2(i)})/N_M$, where $I_{S1(i)}$ and $I_{S2(i)}$ are the star and delta winding currents in the main transformer, the phase to neutral voltage at the output of the star secondary (V_i'') is

$$\begin{aligned} V_i'' &= \frac{V_i'}{N_M} + X_S \frac{dI_{S1(i)}}{d\omega t} \\ &= \frac{V_i}{N_M} + \frac{X_T}{N_M^2} \frac{d}{d\omega t}\left(I_{S1(i)} + \sqrt{3}\, I_{S2(i)}\right) + X_S \frac{dI_{S1(i)}}{d\omega t} \end{aligned} \tag{3-2}$$

Similar arguments apply for the delta output, but in this case the phase to neutral voltage on the primary is converted to a phase to phase voltage in the delta output (V_i'''), where

$$\begin{aligned} V_i''' &= \frac{\sqrt{3}\, V_i'}{N_M} + X_D \frac{dI_{S2(i)}}{d\omega t} \\ &= \frac{\sqrt{3}\, V_i}{N_M} + \frac{\sqrt{3}\, X_T}{N_M^2} \frac{d}{d\omega t}\left(I_{S1(i)} + \sqrt{3}\, I_{S2(i)}\right) + X_D \frac{dI_{S2(i)}}{d\omega t} \end{aligned} \tag{3-3}$$

The switching of the main convertor means that 12 combinations of ac voltages are applied to the dc circuit. It can be shown that the reinjection voltage is repetitive for each main convertor conduction interval, therefore, the discussion is simplified by considering a single main convertor conduction interval, where the dc voltages (V_{B1} and V_{B2}) are defined as

$$\begin{aligned} V_{B1} &= V_R'' - V_B'' \\ V_{B2} &= -V_B''' \end{aligned} \tag{3-4}$$

During any of the main convertor conduction intervals the ac currents consist of the dc current with the reinjection current superimposed. Assuming that the dc current has no ripple, this component does not modify the circuit voltages during this interval and is neglected. The direction of the reinjection current in the ac circuit is defined in figure 3-8, whereby $I_{S1(R)} = -N_R I_{RJ}$ and $I_{S1(B)} = N_R I_{RJ}$. The current flow in the delta configuration is distributed

amongst all three windings, with the requirement that

$$N_R I_{RJ} = I_{S2(Y)} - I_{S2(B)}$$
$$\sum_{R,B,Y} V_i''' = 0 \qquad \textbf{(3-5)}$$

Assuming the impedances are balanced between phases, it can be shown that $I_{S2(B)} = -2/3\ N_R I_{RJ}$ and $I_{S2(Y)} = I_{S2(R)} = 1/3\ N_R I_{RJ}$.
Using equations (3-2), (3-3) and (3-4), along with the ac currents specified in terms of reinjection current, the dc voltage at each main bridge become

$$V_{B1} = \frac{V_R - V_B}{N_M} + \frac{X_T}{N_M^2}\frac{d}{d\omega t}N_R I_{RJ}\left((-1+\sqrt{3}\frac{1}{3}) - (1-\sqrt{3}\frac{2}{3})\right) + X_S\frac{d}{d\omega t}N_R I_{RJ}(-1 - 1)$$

$$V_{B2} = -\sqrt{3}V_B - \frac{\sqrt{3}X_T}{N_M^2}\frac{d}{d\omega t}N_R I_{RJ}\left(1 - \sqrt{3}\frac{2}{3}\right) - X_D\frac{d}{d\omega t}N_R I_{RJ}\left(-\frac{2}{3}\right) \qquad \textbf{(3-6)}$$

The reinjection scheme connects to the main bridges as shown in figure 3-9. Each dc voltage (V_{B1} and V_{B2}) appear across a series combination of blocking capacitor and reinjection transformer. The latter is represented as an ideal transformer with a leakage reactance (X_{RJ}) connected in series on the primary side.

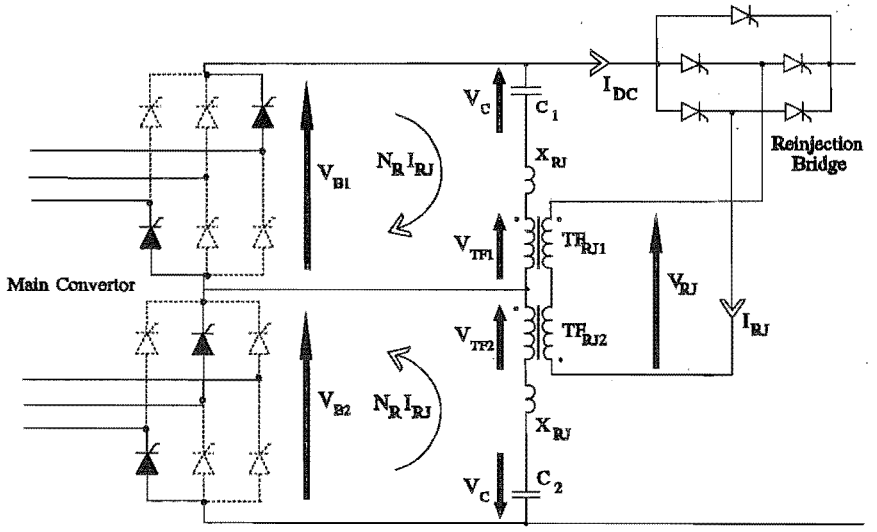

Figure 3-9: Connection of the reinjection scheme to the dc circuit.

The interconnection of the two reinjection transformers is such that its output (V_{RJ}) is given by

$$V_{RJ} = N_R(V_{TF1} - V_{TF2}) = N_R\left[(V_{B1} - V_{B2}) - 2V_C^* - 2X_{RJ}N_R\frac{dI_{RJ}}{d\omega t}\right] \quad \textbf{(3-7)}$$

where V_{TF1} and V_{TF2} are the reinjection transformer voltages and V_C^* is the 6^{th} harmonic component of the blocking capacitor voltage. V_C^* is defined by

$$V_C^* = \frac{1}{\omega C}\int N_R I_{RJ}\, d\omega t \quad \textbf{(3-8)}$$

Using equation (3-6), (3-7) and (3-8), V_{RJ} becomes

$$V_{RJ} = N_R\left[\frac{V_R + V_B(\sqrt{3}-1)}{N_M} - 2\left(\frac{X_T}{N_M^2}(2-\sqrt{3})+X_S+\frac{X_D}{3}+X_{RJ}\right)N_R\frac{dI_{RJ}}{d\omega t} - \frac{2N_R}{\omega C}\int I_{RJ}d\omega t\right] \quad \textbf{(3-9)}$$

An equivalent circuit representation of equation (3-9) is shown in figure 3-10, consisting of a voltage source (V_{com}) and capacitive and inductive reactances defined at the fundamental frequency (X_C and X_{RC}). This configuration is similar to the conventional ac/dc convertor with series connected capacitor (Reeve *et al.*, 1968; Neiman *et al.*, 1967) and the analysis of its commutations provide useful insight into the operation of the reinjection scheme. With the ac supply voltages defined as $V_R = N_M(V_1/\sqrt{3})\ \angle 30$, $V_B = N_M(V_1/\sqrt{3})\ \angle -90$ and $V_Y = N_M(V_1/\sqrt{3})\ \angle +150$ the commutating voltage (V_{com}) is

$$V_{com} = N_R\left(\frac{V_R + V_B(\sqrt{3}-1)}{N_M}\right) = \sqrt{2-\sqrt{3}}\ N_R V_1\ \angle -15° \quad \textbf{(3-10)}$$

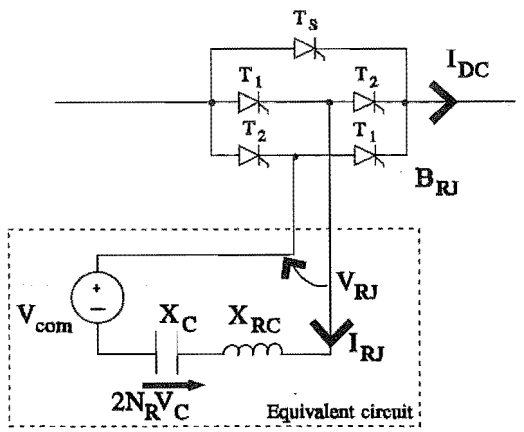

Figure 3-10: Equivalent circuit of the reinjection scheme.

In other words, V_{com} is $\sqrt{2}\sqrt{2-\sqrt{3}}\ N_R V_1 \sin(\omega t - 15°)$ defined over one main bridge conduction interval ($\alpha < \omega t < \alpha+30°$).

From equation (3-9) the reactances of the equivalent circuit are defined as

$$X_{RC} = 2N_R^2\left(\frac{X_T}{N_M^2}(2 - \sqrt{3}) + X_S + \frac{X_D}{3} + X_{RJ}\right) \qquad \textbf{(3-11)}$$

$$X_C = 2N_R^2\left(\frac{1}{\omega C}\right)$$

3.5.2 Reinjection bridge commutation with a small blocking capacitor

The 6th harmonic component of the capacitor voltage, defined in equation (3-8), is illustrated in figure 3-11(b) using measured waveforms from the hardware model when it is operating with a dc current of 6.8 A. The phase of this voltage is such that it is maximum

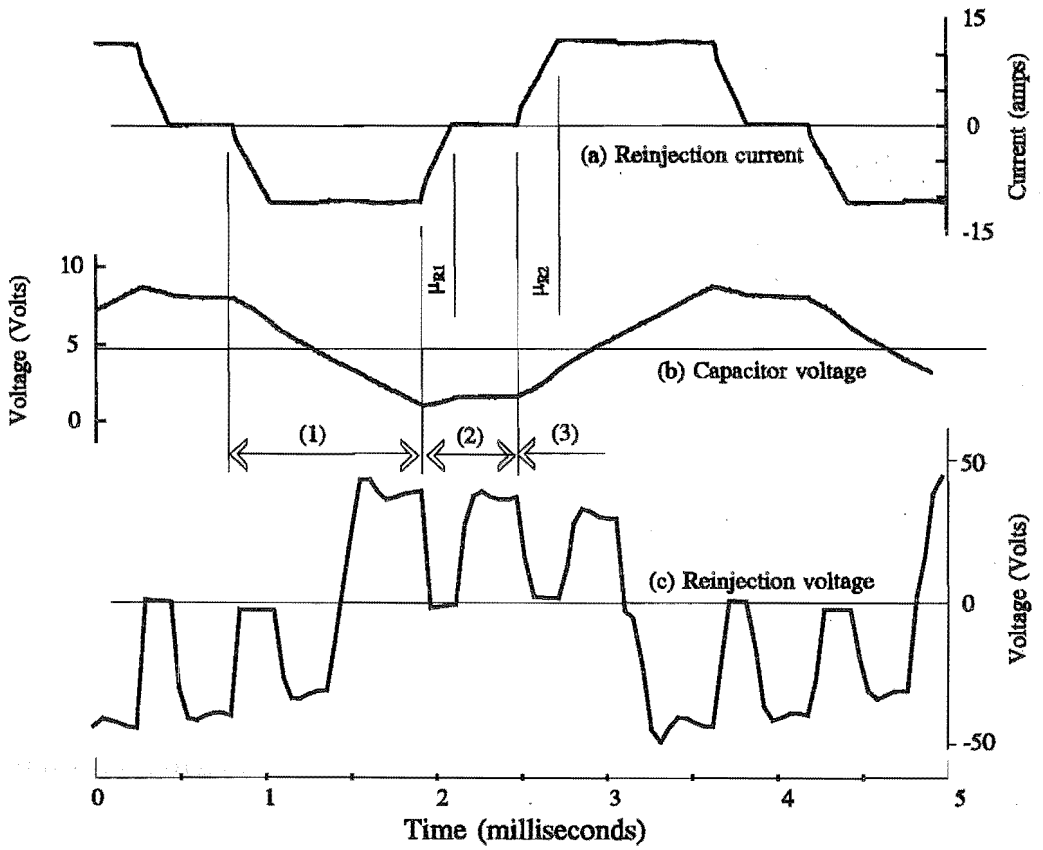

Figure 3-11: The relationship between capacitor voltage magnitude and commutations.

approximately at the same time for the first and second reinjection bridge commutations. As an example, a main bridge conduction interval is selected and the corresponding reinjection bridge commutation intervals are identified by μ_{R1} and μ_{R2}, as shown in figure 3-11. In these intervals the commutating voltage is positive, the capacitor voltage is negative (figure 3-11(b)) and V_{RJ} equals zero (figure 3-11(c)), resulting in the voltage across the inductance being increased because of the capacitor voltage. Hence, the duration of both commutations become shorter by a similar factor.

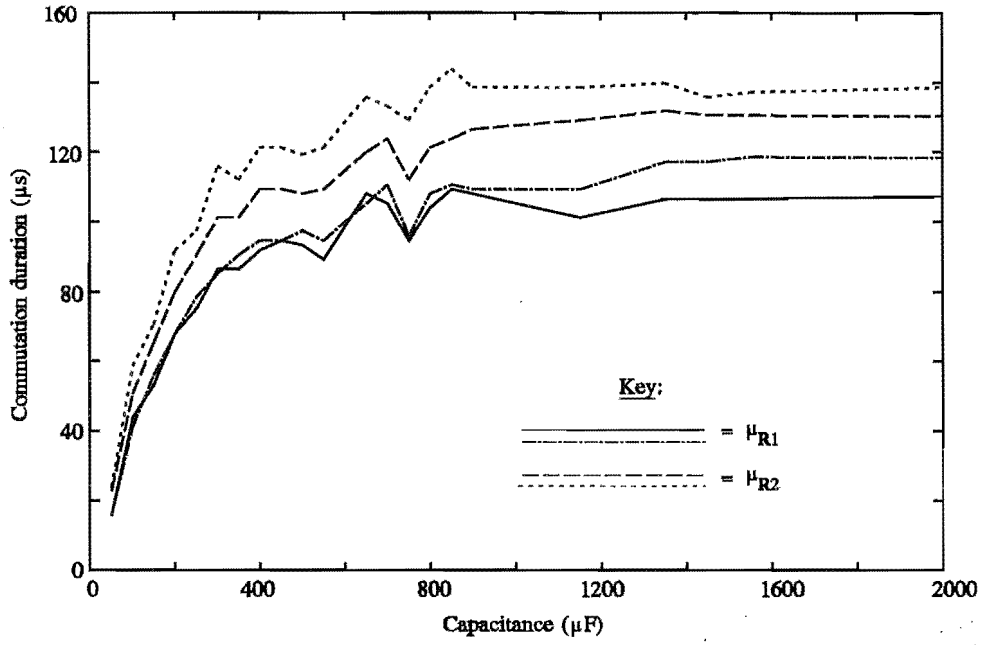

Figure 3-12: Variation of reinjection bridge commutation interval with blocking capacitor size.

The variation of reinjection bridge commutation intervals when the capacitor size is changed is shown in figure 3-12. The capacitor becomes significant (i.e. begins to modify the commutations) at approximately 800 μF. The change in commutation duration is also dependent on the level of dc current flowing and rated dc current causes the commutation interval to begin changing at 1600 μF. This is approximately equal to the capacitor value specified by the criteria in chapter 2. In other words, the capacitor voltage is significant when this size specification is used.

3.5.3 Reinjection bridge commutation with a large blocking capacitor

When the blocking capacitors are large and the 6^{th} harmonic component of the capacitor voltage is insignificant, the last term in equation (3-9) is neglected. From this equation the

two reinjection bridge commutations are simplified to

$$\int_{\alpha+10°}^{\alpha+\mu_{R1}+10°} \sqrt{2}\sqrt{2-\sqrt{3}}\ V_1 N_R \sin(\omega t - 15)\, d\omega t = X_{RC}\int_{I_{DC}}^{0} dI_{RJ}$$

$$\int_{\alpha+20°}^{\alpha+\mu_{R2}+20°} \sqrt{2}\sqrt{2-\sqrt{3}}\ V_1 N_R \sin(\omega t - 15)\, d\omega t = X_{RC}\int_{0}^{I_{DC}} dI_{RJ} \qquad \textbf{(3-12)}$$

(assuming no resistance in the circuit). By virtue of the firing angle being near 90° and the commutation duration being small, equation (3-12) becomes

$$\cos(\alpha-5°) - \cos(\alpha-5°+\mu_{R1}) = \frac{X_{RC}I_{DC}}{N_R\sqrt{2}\sqrt{2-\sqrt{3}}\ V_1} \approx \mu_{R1}$$

$$\cos(\alpha+5°) - \cos(\alpha+5°+\mu_{R2}) = \frac{X_{RC}I_{DC}}{N_R\sqrt{2}\sqrt{2-\sqrt{3}}\ V_1} \approx \mu_{R2} \qquad \textbf{(3-13)}$$

This shows that the two commutations in the reinjection bridge are approximately equal. With reference to the hardware model, the blocking capacitor is 1500 μF, large enough to be able to neglect the effects of the capacitor at the current level in these tests. The commutation intervals of the reinjection bridge (μ_{R1} and μ_{R2}) are either 107 and 131 μs, respectively, or 123 and 138 μs, respectively, (given a 5% measurement error) depending on the polarity of the reinjection voltage. The commutation voltage is different for each polarity, originating from a voltage imbalance between the two main bridges, giving rise to the asymmetric commutation intervals. Also note that, in either case, μ_{R1} does not equal μ_{R2} as predicted by equation (3-13). This discrepancy occurs because of the resistances inherent in the circuit. These resistances are significant in the hardware model and their presence decreases the duration of the first commutation and increases the second, and is described in more detail in section 3.5.5.

Using equation (3-13) and measured parameters from the hardware model, the theoretical value for the reinjection bridge commutation interval (μ_{R1}=μ_{R2}) is 138 μs (given an 18% error). From figure 3-12, when the blocking capacitor is large, it is evident that the measured values of commutation interval are all contained within the region of error of the theoretical value, supporting the validity of equation (3-13).

Equation (3-11) shows that changes in (X_T/N_M^2) has less effect on X_{RC} than the other reactances in the circuit. This is confirmed by adding extra reactances to the hardware model so that the values of X_T and X_{RJ} are changed by ΔX_T and ΔX_{RJ}, respectively. Theoretically, it is shown in equation (3-13) that the increase in μ_{R1} or μ_{R2} (i.e. both are approximately

equal to $\Delta\mu_R$) because of ΔX_T or ΔX_{RJ} are given by

$$\Delta\mu_R = \frac{\sqrt{2}\left(\frac{\Delta X_T}{N_M^2}(2-\sqrt{3})\right)I_{DC}}{\sqrt{2-\sqrt{3}}\,V_1} \qquad \textbf{(3-14)}$$

$$\Delta\mu_R = \frac{\sqrt{2}\left(\Delta X_{RJ}\right)I_{DC}}{\sqrt{2-\sqrt{3}}\,V_1}$$

From equation (3-14) the rate of change of $\Delta\mu_R$ with respect to ΔX_{RJ} is $1/(2-\sqrt{3})$ times larger than the rate of change of $\Delta\mu_R$ with respect to $(\Delta X_T/N_M^2)$. From the hardware model the measured μ_R as a function of ΔX_{RJ} or $(\Delta X_T/N_M^2)$ (e.g. $\mu_R=f(\Delta X_{RJ})$) is shown in figure 3-13. The rate of change of μ_R with respect to the added reactances (either ΔX_T or ΔX_{RJ}) is 145 μs/ohm and 669 μs/ohm, respectively. The ratio of these values is 0.216. The difference between measured and theoretical values is within the bounds of experimental error and it is concluded that the measurements support the theory.

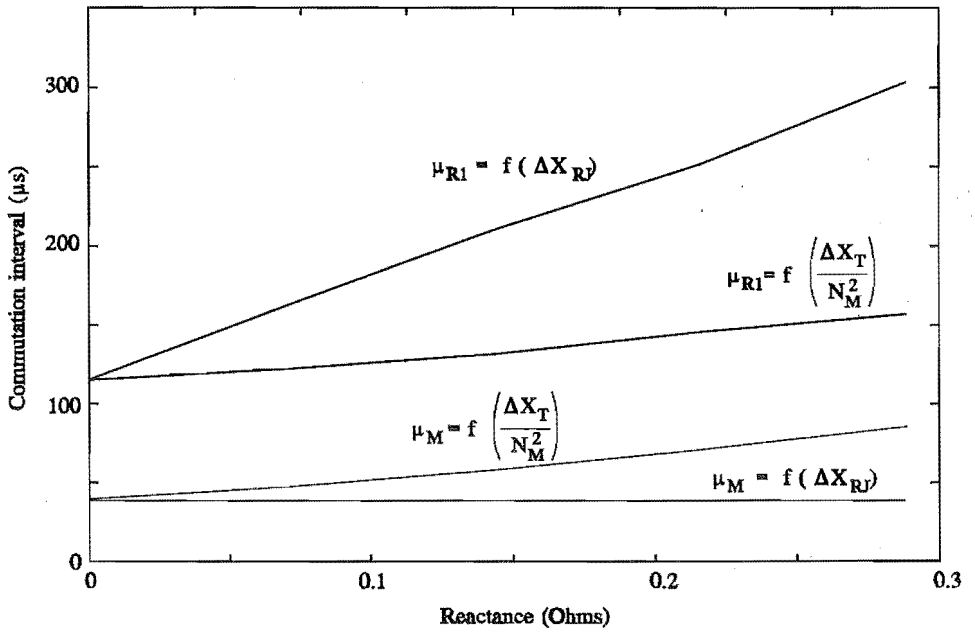

Figure 3-13: Measured commutation intervals when X_T or X_{RJ} are increased.

3.5.4 Equalising the main and reinjection bridge commutations

To force the main and reinjection bridge commutation intervals to be equal, the size of both the capacitive and inductive reactances in the commutating circuits must be reconsidered. When the hardware model is operated at 6.8 amps, the 6^{th} harmonic component of the capacitor voltage is insignificant. In this case, the main and reinjection bridge commutation intervals are specified by equations (2-2) and (3-13), respectively. From equation (2-2), the commutation interval for the main convertor (μ_M) is

$$\mu_M \approx \frac{\sqrt{2}X_{MC}(1-N_R)I_{DC}}{V_1} \qquad \textbf{(3-15)}$$

When μ_M,μ_{R1} and μ_{R2} are forced to be equal, it can be shown that the commutating reactances are related by

$$\sqrt{2}X_{MC}(1-N_R) = \frac{X_{RC}}{N_R\sqrt{2}\sqrt{2-\sqrt{3}}} \qquad \textbf{(3-16)}$$

In other words, $X_{MC} = 3.72X_{RC}$. Given that $X_{MC} = \frac{X_T}{N_M^2} + X_S$, and using equation (3-11), then

$$\frac{X_T}{N_M^2} = 977\left(1.7X_S + X_{RJ}\right) \qquad \textbf{(3-17)}$$

Equation (3-17) shows that X_S and X_{RJ} must be three orders of magnitude smaller than X_T/N_M^2. For example, with X_T= 100%, X_S and X_{RJ} are in the order of 0.03%. Stigant *et al.* (1973) discusses how transformers have been made with leakage reactances as low as 2%, but 5% is more common. Hall *et al.* (1990) state that a typical parallel connected 12-pulse ac/dc convertor uses a transformer with primary leakage reactance of 10% and secondary leakage reactances of 2% to help maintain balanced operation. These leakage values suggest that 0.03% leakage reactance is not practical without a specialised design, implying significantly increased cost. For the hardware model a single main transformer is used, configured with a single primary and two secondaries to provide the smallest possible leakage reactance between secondary windings. Even with minimised leakage reactance the commutation interval of the main convertor is approximately 45 μs, whereas the average commutation interval of the reinjection bridge is 125 μs, i.e. a factor of 2.8 different. Applying the measured values of X_S and X_{RJ} (0.08 and 0.06, respectively) into equation (3-17) shows that (X_T/N_M^2) must be 215 Ω to balance the commutations. The measured value of (X_T/N_M^2) is 0.33 Ω, significantly smaller than required, and correlates with the commutation interval mismatch.

When X_T is increased by ΔX_T, as illustrated in figure 3-13, the rate of change of the μ_M is 145 μs/ohm and the rate of change of μ_{R1} is 160 μs/ohm. Knowing that μ_M and μ_{R1} are nominally 45 and 110 μs, respectively, the commutation intervals will converge when X_T equals 4.3 ohms. This value is an order of magnitude larger than the hardware model value, but is two orders of magnitude smaller than expected by theory. Given the similarity in rate of change of commutation intervals and their possible measurement error, a good match is unlikely. In overview, it is concluded that the trend supports the theory (i.e. X_T must be large).

An alternative to increasing the value of X_T in order to equalise the commutations is to have a small blocking capacitor. Figure 3-12 shows that the reinjection bridge commutation interval decreases when the blocking capacitor size is decreased. Moreover, the main bridge commutation is unaffected by the blocking capacitor. Therefore, the hardware model commutations are balanced at 45 μs when the capacitor is approximately 100 μF. The peak reverse voltage requirements for the reinjection bridge are significantly increased, as discussed in chapter 2, hence there is a compromise between commutation balancing and increased cost of the reinjection bridge.

3.5.5 Reinjection bridge commutation with resistance present

The equivalent circuit for the reinjection scheme, shown in figure 3-10, does not include any resistances that are inherent in the compensator's components. This is because they are negligible in high power schemes. It is not the case in the hardware model, however, and it is the purpose of this section to give an overview of their effect on the compensators operation and the hardware results.

For this discussion it is assumed that the blocking capacitor is negligible and the commutating impedance consists of an inductive reactance and resistance (R_{RC}) only.

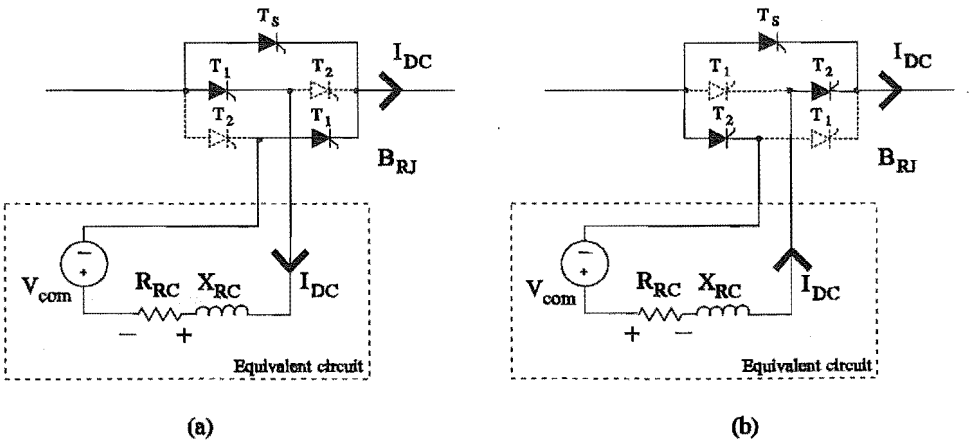

Figure 3-14: Simplified reinjection circuit during commutations.

In a given conduction interval of the main convertor there are two reinjection bridge commutations, as illustrated with the two simplified reinjection circuits in figure 3-14.
In the first commutation, shown in figure 3-14(a), thyristors T_1 and T_S are conducting and the polarity of the voltage generated across the resistance (because of the reinjection current) and the commutating voltage are indicated. The reinjection voltage is zero, forcing the voltage across the reactance to be increased because of the resistance. The net effect is a reduction in commutation interval.
In the second commutation, shown in figure 3-14(b), the flow of the dc current in the equivalent circuit has changed direction and the voltage generated across the resistance decreases the voltage across the reactance. The net effect is the opposite to the first case, i.e. the commutation interval is longer. This is confirmed experimentally by adding resistance to the hardware model on the secondary side of the reinjection transformer. The resulting commutation intervals of the first reinjection bridge commutation are shown in figure 3-15. From equation (3-13), when the resistance is approximately zero, the reinjection bridge commutation intervals are equal. Therefore, extrapolation of the commutation interval traces (shown in dotted lines in the figure) shows that approximately 0.5 ohms of resistance is inherent in the circuit.

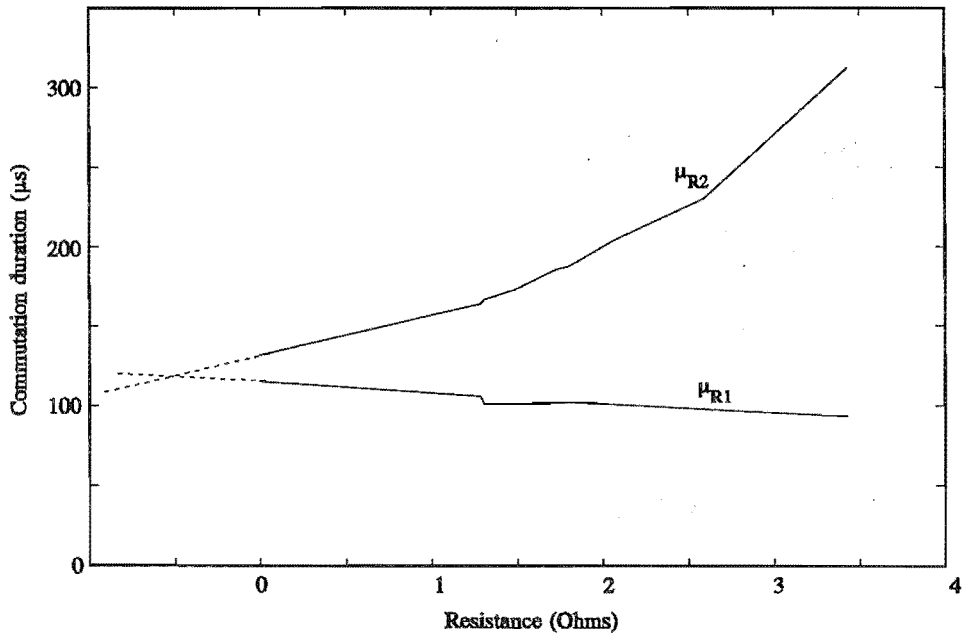

Figure 3-15: Variation of the reinjection bridge commutation intervals with different resistance

3.6 Conclusion

A 2.6 kVAr hardware model of the proposed scheme is constructed and is controlled by a digital signal processor. The complete control structure is implemented in the processor, not only giving precise firing for the thyristors, but also providing capacity for complex control structures.

Measured voltage and current waveforms confirm the predicted operation of the ac/dc conversion process, whereby both the ac current and dc voltage waveforms have a 36 pulse characteristic, given that the hardware model contains symmetries and scale-down discrepancies, with respect to time constants and magnetisation nonlinearities. Moreover, the experimental results have clearly shown the ability of the proposed configuration to absorb controllable reactive power while maintaining 36-pulse operation.

The steady state and dynamic criteria for dc reactor size (in chapter 2) do not prevent dc side harmonics from appearing in the ac current, but this is only a problem when the blocking capacitor size is significantly less than the criteria from chapter 2. A difference in main and reinjection bridge commutation intervals also modifies ac current harmonics levels (as well as modifying the operating characteristic). An expression describing the reinjection bridge commutation is derived, neglecting the blocking capacitor, and is validated with measured results. This shows that it is difficult to implement the transformers with low enough leakage reactances to achieve equal commutation intervals. However, the blocking capacitor can be utilised to equalise the commutations, but at the expense of creating dc side harmonics.

Chapter 4

Software modelling

Software modelling is the second technique used in this thesis to illustrate the operation of the proposed scheme, the first technique being the hardware modelling described in chapter 3. The need to perform dynamic studies combined with the presence of thyristor switchings in the compensator, implies that time domain simulation is the most effective analysis method (Arrillaga, 1990). Currently, state variable and electromagnetic transient based programs are commonly available, whereby the latter is the basis to the software modelling in this thesis. The package used is called EMTDC-PSCAD (Manitoba HVDC, 1988; Woodford *et al.*, 1983) and it has the advantage that there are extensive libraries enabling the precise modelling of the compensator, as well as comprehensive modelling of the power system. The modelling technique (i.e. EMTDC) is well proven with years of use, but the components for the compensator are configured in a way that is unique, and validation of their combined operation is necessary.

In this chapter a high power model of the compensator is developed suitable for implementation into a high voltage ac system. Its steady state operation is tested by comparing measured waveforms and operating characteristics with theory. Since this model is destined to demonstrate the dynamic characteristics of the compensator, its controller design is described in detail. This is because the controller is an integral part of the compensator's response. The compensators response is illustrated in several dynamic situations, giving an appreciation for the limitations of the controller design.

4.1 Simulation validation

EMTDC has been used for many years, particularly in the study of HVDC transmission. Consequently, there are many papers describing the use of Graetz bridge models (an example is Woodford, 1985), giving confidence in the correct operation of the compensator's main convertor. The model of the reinjection scheme, however, uses components in a way that is unique, requiring their combined operation to be validated. The validation method consists of duplicating the hardware model, discussed in chapter 3, in the simulation package, using component values listed in Appendix A. Examples of results from both models are superimposed in figures 4-1, 4-2 and 4-3, to illustrate the model comparison.

The ac current for both models (figure 4-1) is compared by way of their harmonic content, and good agreement is observed, except at the low harmonic orders, which is attributed to transformer magnetisation and ac phase imbalances. The magnetisation of the software transformers is linearised, therefore the ac current of the software model lacks any magnetising current harmonics. Moreover, voltage and impedance imbalances between phases are not represented in simulation, giving rise to a significant difference in the 3^{rd}, 5^{th} and 7^{th} harmonics.

The 12-pulse dc voltage waveforms (figure 4-2) show good agreement, illustrating that the approximations made in the ac generator modelling are adequate. The generator is represented as a voltage source in series with an impedance, where the oversimplified frequency

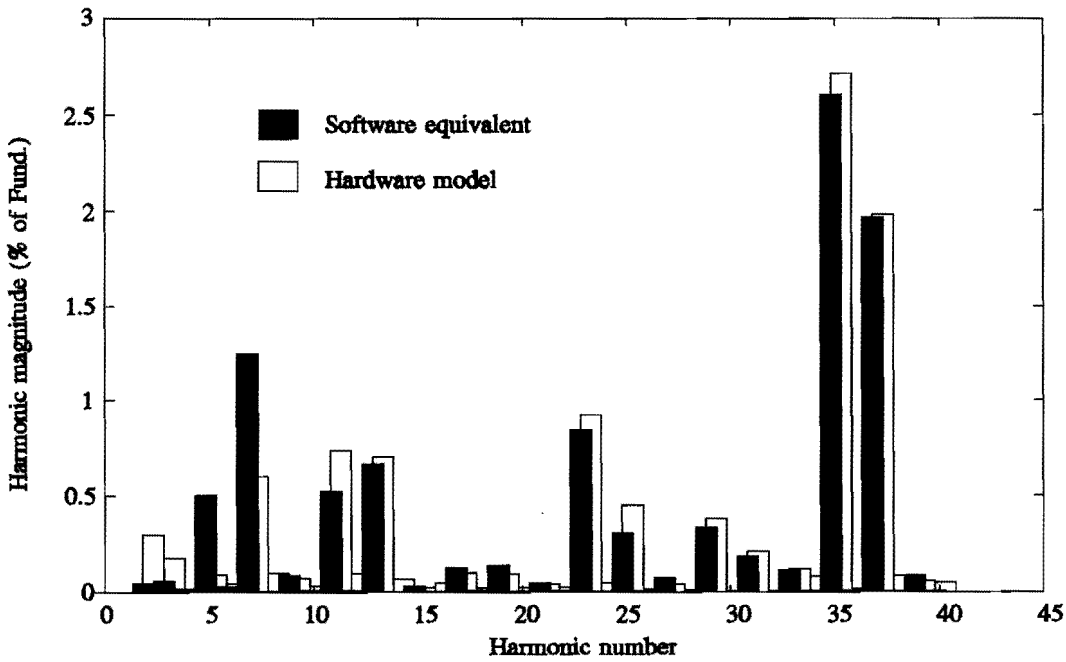

Figure 4-1: Comparison between hardware and software equivalent - ac current harmonic content.

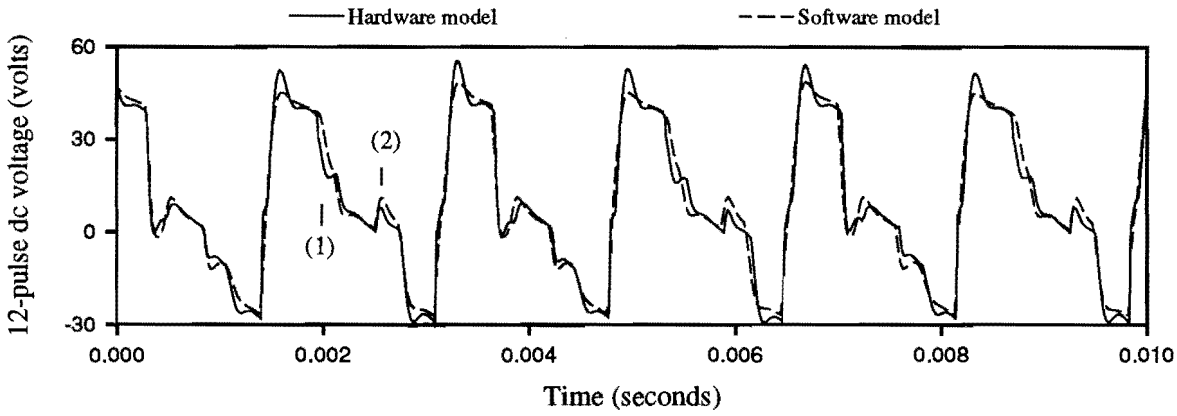

Figure 4-2: Comparison between hardware and software equivalent - 12-pulse dc voltage.

dependence of the impedance only causes minor errors in the trends of the voltage waveforms. In particular, the voltage appears more damped than the hardware model waveforms. Furthermore, the choice of series impedance results in similar convertor operation, as observed when the reinjection bridge commutation intervals are compared (see features (1) and (2) in the figure).

The third example illustrates the dynamic response of the compensator model in the event of a step change in firing angle (89° to 85°). Figure 4-3 depicts the voltage across the blocking capacitor from both models, where a filter is used to attenuate the 6^{th} harmonic component leaving the low frequency LC oscillation (between the blocking capacitor and reinjection transformer magnetising inductance). Both waveforms have similar oscillation frequencies, indicating that the magnetising inductance of the hardware model reinjection transformer is

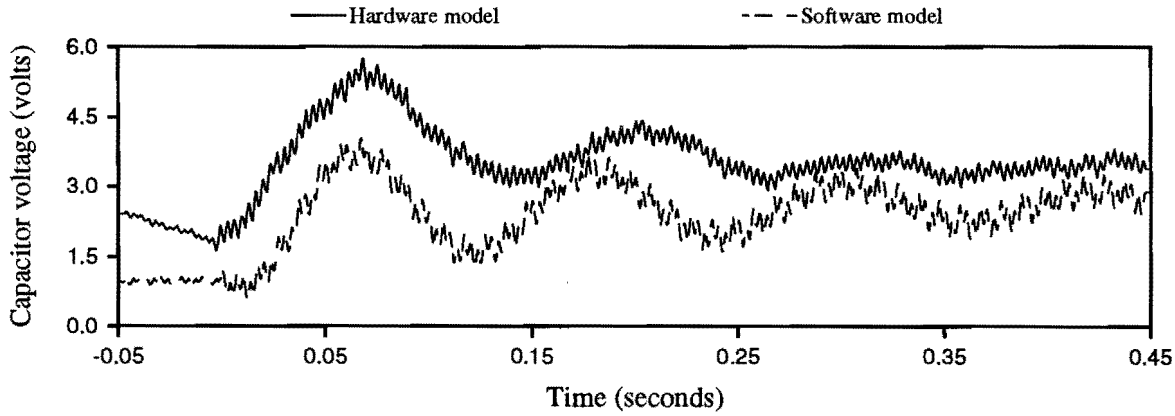

Figure 4-3: Comparison between hardware and software equivalent - capacitor voltage during a step change in firing angle

approximately linear, as is the case for the software equivalent.
There is a difference in the initial steady state dc level (before 0 seconds in figure 4-3), relating to a difference in resistance distribution in the circuit. This correlates with the damping of the oscillation being higher in the hardware model.

4.2 Description of the high power software model

Having validated the software modelling techniques in section 4.1, the representation is scaled up to a high power level, suitable for application into an ac system at high voltage. The component ratings for the high power compensator model are all specified using the criteria described in section 2.3. These criteria require a VA rating for the compensator (Q), which is chosen based on the ac system environment. Variation in 220 or 275 kV transmission voltages, caused by variation in the ac power flow, are such that SVCs are typically rated between approximately 50 to 150 MVAr (Thanawala, 1985; Baker *et al.*, 1992; Lowe, 1989). For the software model, a 100 MVAr rating is chosen for operation in a 220 kV system. Furthermore, the ac voltage at the main transformer secondary (V_1) is dictated by the capabilities of the thyristors used. Recently installed thyristor based compensators use devices with ratings of the order of 2 to 4 kA and 4 to 6 kV. They are stacked in series for operation at approximately 10 to 20 kV (typical examples are described in Tyll *et al.*, 1993; Al-Baya *et al.*, 1993). With consideration to safety margins, the proposed compensator current rating is defined with respect to a dc current rating of 1.5 kA, which fixes V_1 at 25 kV. From these ratings the dc reactor value is 100 mH, assuming the dynamic criteria described in chapter 2 are used, and the blocking capacitor value is 582 μF.
In the following sections simulation results are used to illustrate aspects of its steady state operation when the software model is connected to a simplified representation of the power system, i.e. a constant ac voltage source in series with a reactive impedance. The results are separated into time domain waveforms obtained from within the compensator and operating characteristics with respect to the control of reactive current. Both these aspects expand the confidence in the results already gained with the hardware model, discussed in chapter 3.

4.2.1 Simulated waveforms

With a dc current of 1.125 kA, the software model produces voltage and current waveforms as shown in figures 4-4 and 4-5, respectively. These figures show a good agreement with theoretical (discussed in section 2.1) and hardware model waveforms (discussed in section 3.2). For example, both the hardware and software model results show similar commutation

notches in the reinjection voltage. Unlike the hardware model, however, the software model is design by specifying the transformer reactances and ac voltages associated with each main bridge to be equal, resulting in each bridge producing equivalent dc voltages (figure 4-4(a)). Consequently, the 12-pulse dc voltage is not modified during the reinjection bridge commutations as specified by the theory (see feature F-II in figure 4-4(c)).

With respect to the duration of the reinjection bridge commutations, 112 and 115 μs are measured from the waveforms. Being approximately equal, these values confirm that the resistances in the software model have negligible effect on the reinjection bridge commutations, as discussed section 3.5.5. From equation (3-13) the theoretical value of commutation interval is 137 μs (as calculated using the data from Appendix B). When the blocking capacitor is increased in size (i.e. 1 F), the measured intervals increase to 133 and 135 μs. The similarity of the software model commutation intervals (when the capacitor is large) and the corresponding theoretical values gives sound validation of the reinjection bridge commutation theory.

In the design of the software model, the duration of the reinjection bridge commutation is adjusted by selecting suitable values for the leakage reactances associated with the secondary windings of the main transformer and reinjection transformers. These reactances are minimised (to practical levels) in an attempt to equalise the duration of the main and reinjection bridge commutations, as discussed in section 3.5.4. The main bridge commutation interval in the simulated waveforms is 90 μs, which is smaller than the reinjection bridge commutation. This shows that the difference between the main and reinjection bridge commutation intervals will not be eliminated by adjusting leakage reactances alone. The above results illustrate, however, that a finite blocking capacitor size reduces the reinjection bridge commutation interval and this effect must also be taken into consideration.

4.2.2 Operating Characteristics

The most significant changes in ac current fundamental magnitude and harmonic content occur between approximately 50° and 90°, as shown in figure 4-6. The time domain waveforms used to generate this figure confirm that three modes of operation exist over the firing angle range mentioned above. From 90° to approximately 89.5° the dc current is discontinuous, commutation does not occur and this is called discontinuous mode. The current magnitude is insignificant compared to rated current and this mode is neglected. Between approximately 89.5° and 82° the compensator is in single commutation mode, and below 82° the commutations overlap, invoking the multiple commutation mode. The transition between single and multiple commutation modes (α_{mt}, occurring at approximately 82°) is illustrated in the figure as a sudden change in slope of the fundamental trace (I_1) and a sudden rise in

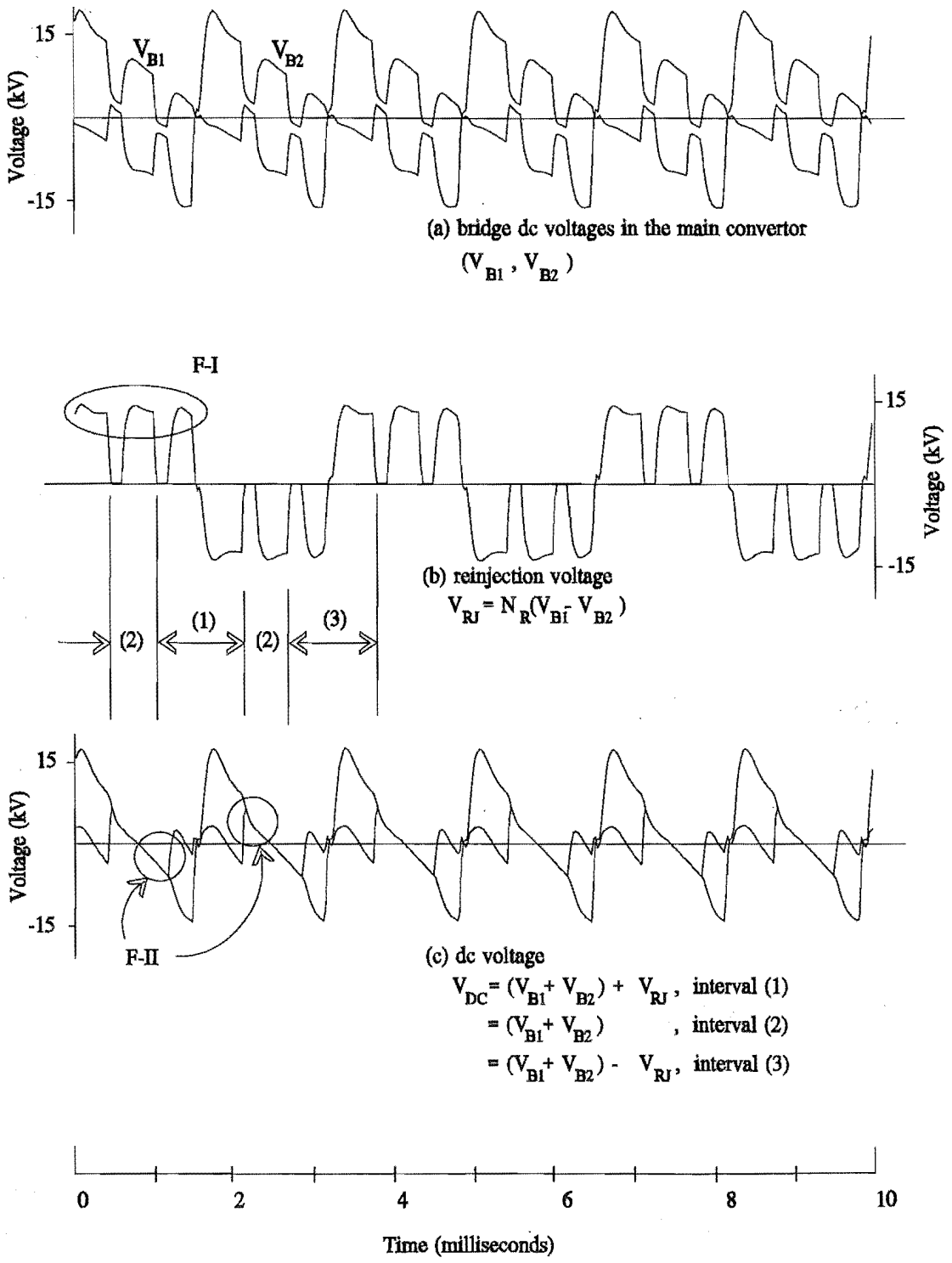

Figure 4-4: Measured voltage waveforms from the software model.

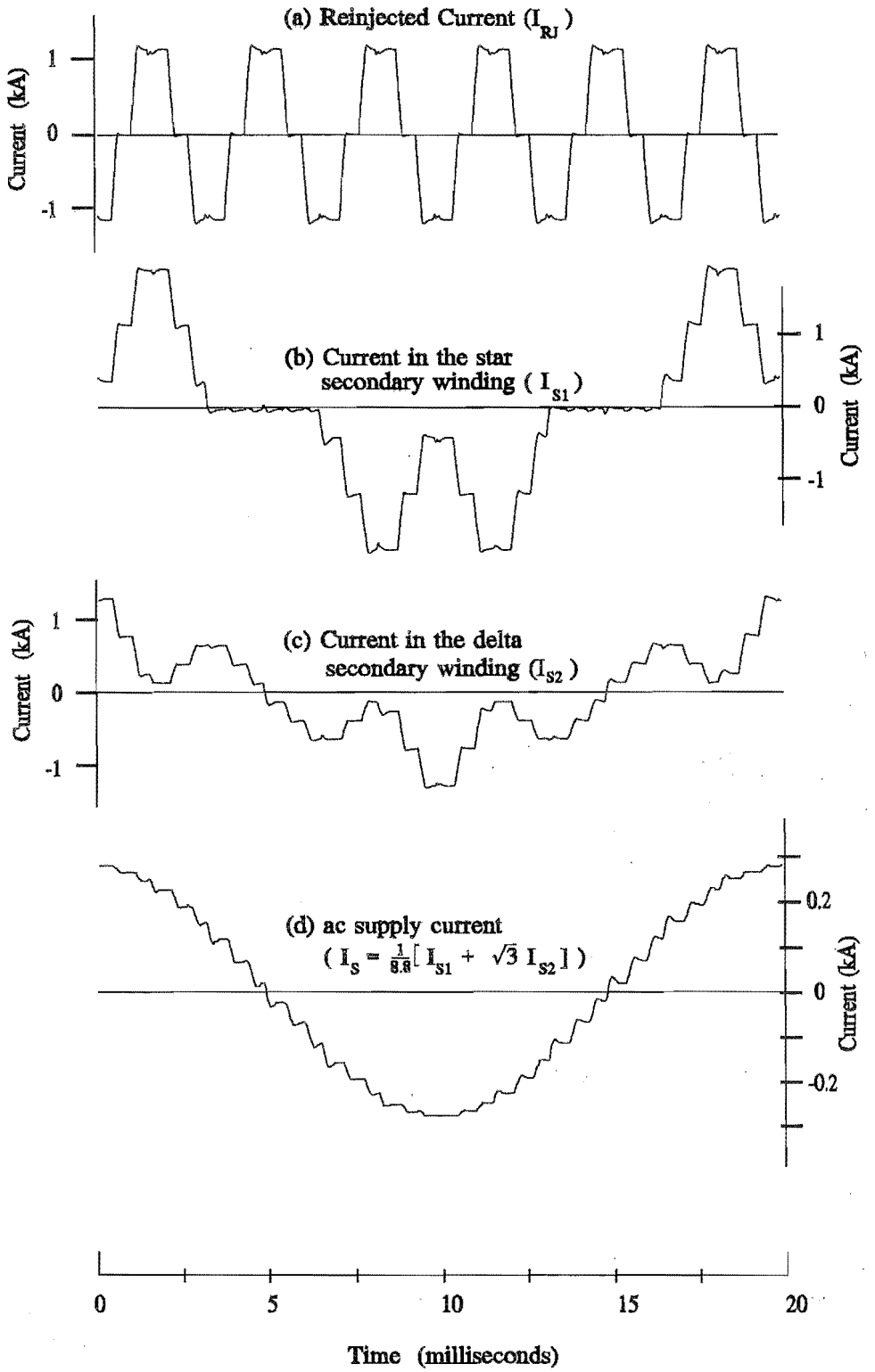

Figure 4-5: Measured current waveforms from the software model.

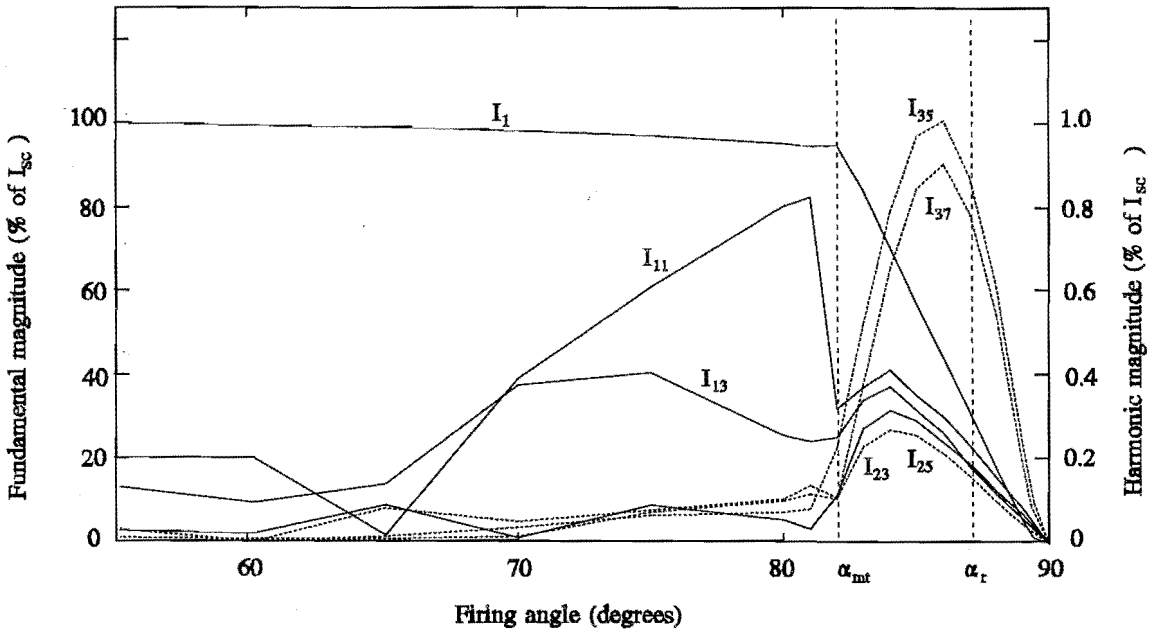

Figure 4-6: Characteristic of the simulation model

the 11^{th} harmonic as the reinjection scheme ceases to operate correctly.

The firing angle range of the single commutation mode is 3° larger than the ideal case shown in figure 2-7, suggesting that the current limiting resistances in the software model, shown in equation (2-1) as $R+K_eX_{MC}$, are larger than the ideal. The commutating resistance (K_eX_{MC}) is specified in terms of the main bridge commutating reactance under the assumption that the main and reinjection bridge commutation intervals are equal. When the reinjection bridge commutation interval is larger than the main bridge, as is the case with the software model, the commutating resistance is larger than expected. Equations (2-2) and (3-13) specify these commutating intervals, which are used in conjunction with equation (2-7) to modify the definition of K_e to

$$K_e \approx \frac{6}{\pi}\left[(1-N_R)^2 + \frac{X_{RC}}{X_{MC}}\right] \qquad \textbf{(4-1)}$$

In the software model the commutating resistance is increased from the ideal of 1.05 Ω to approximately 1.25 Ω and the resistance inherent in the total circuit is estimated to be approximately 0.45 Ω. As predicted by theory, inherent resistances that are less than the commutating resistance do not significantly affect the maximum current in the single commutation mode (I_{mt}). The measured value of I_{mt}/I_{sc} equals 0.95, whereas the predicted is 0.987. Moreover, the larger firing angle range does not effect the trends in the harmonic content, but does stretch the characteristic in proportion with the operating range change.

4.3 The compensator control structure

Regulation of the ac bus voltage, being a common control objective for compensators (Miller, 1982; Hauth *et al.*, 1982), is the chosen task for the software model. Control structures for this goal usually have a closed loop feedback form, whereby the compensator's reactive current is adjusted depending on the measured ac voltage (Miller, 1982).

In the case of the thyristor controlled reactor, where the voltage controller directly manipulates the firing angle, the voltage control characteristic (shown in figure 4-7) is implemented on the assumption that the firing angle is proportional to the reactive current level. Typically, this uncertainty in current level is removed by measuring the compensator current and feeding it back into the control system. The most common feedback structure adds the measured current signal (scaled) to the measured voltage signal, both being root mean square (RMS) values. This forms a modified voltage signal that is forced to equal the reference voltage by controlling the firing angle (examples are Schweickardt *et al.*, 1978; Romegialli *et al.*, 1981; Frank *et al.*, 1981; Lowe *et al.*, 1990). The scaling of the measured current constitutes the slope of the voltage control characteristic (discussed later in this section). Alternatively, a current controller is nested within the voltage control loop. In other words, the voltage control loop explicitly specifies the desired current level for the current control loop, based on the voltage control characteristic. The current controller changes the firing angle to force the measured current to equal the desired level (Miller, 1982). Mathematically these two feedback structures are equivalent.

The control structure for the NC-SVC is a nested 3 loop negative feedback configuration, as shown in figure 4-8. The control objective is to maintain the ac bus voltage, so the outer most loop is an ac voltage controller. Within the voltage control loop there is a current controller

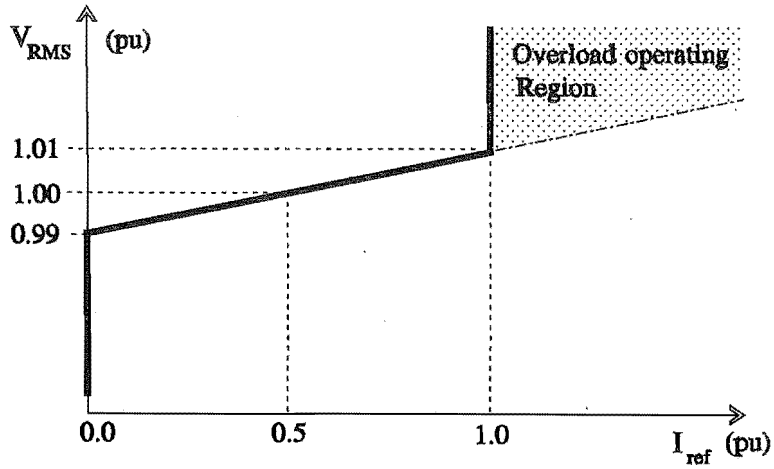

Figure 4-7: Voltage control characteristic.

and within that loop is a thyristor firing pulse synchroniser.

The ac bus voltage control loop is implemented by comparing the true RMS value (V_{RMS}) of the measured ac voltage (value limited between 0.8 and 1.1 pu) with the reference voltage (V_{ref}). The resulting error signal is used by the automatic voltage regulator (AVR) to set a current reference signal (I_{ref}) for the compensator current control loop, according to the AVR characteristic shown in figure 4-7. The AVR must possess a low pass filter to eliminate the noise contained in the voltage signal and in this case a time constant of 50 ms is chosen. This is a disadvantage when large transitions occur, causing large delays, and actual compensator installations usually bypass the AVR during these contingencies (Hauth *et al.*, 1978). In this case, however, these control adjustments are not implemented.

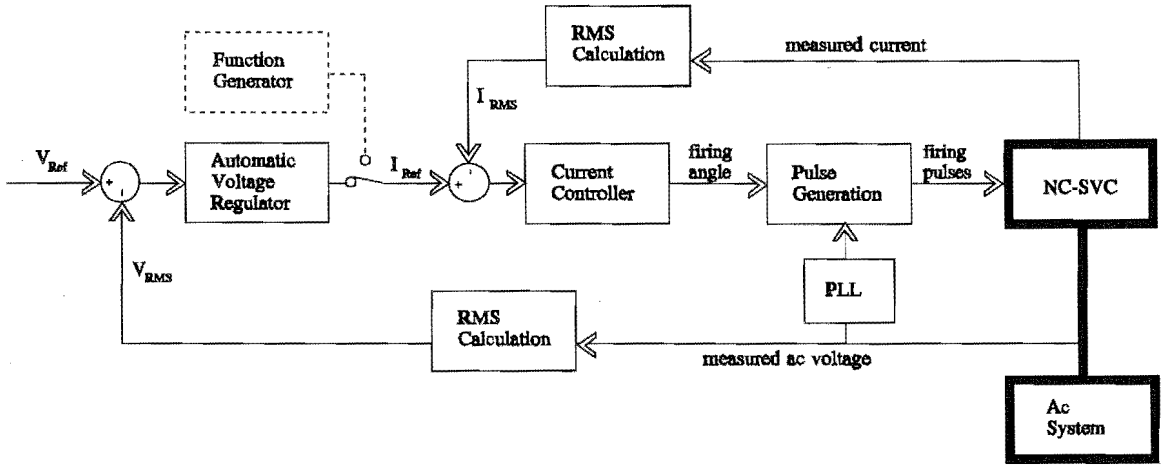

Figure 4-8: Control structure of the software model

The current reference signal is continuously adjustable from 0 to 3 pu, and is magnitude limited outside this region. In the adjustable region, the characteristic is linear and positioned such that at a bus voltage of 1.00 pu the NC-SVC is in the middle of the operating range (i.e. 0.5 pu) and the slope is 2%. This slope represents the gain of the voltage controller and is chosen to avoid instability when the ac system impedance is maximum (i.e. when the system gain is largest) (Schweickardt *et al.*, 1978; Romegialli *et al.*, 1981). To implement the slope characteristic, V_{ref} is assigned the minimum controllable voltage value (i.e. 0.99 pu) and the gain of the proportional controller in the AVR is set to achieve the specified AVR slope.

As mentioned earlier the current controller improves the accuracy of control. In this case both the ac bus voltage control loop and thyristor firing synchroniser have a large time constant, compared to the time constant of a typical ac system disturbance, and the time constant of the dc side impedance within the NC-SVC. A fast current control loop is needed to ensure that the correct current level is maintained in all conditions.

The current control loop is implemented by comparing the RMS value of the measured compensator current (I_{RMS}) with I_{ref}. For the software model the dc current is measured and used as I_{RMS}, since they are proportional and no RMS calculation is necessary. This is assuming that the compensator current is predominantly reactive and extraction of the reactive current component (an example is given in Boyko *et al.*, 1991) is not needed. The error signal from the comparison is processed by the current controller to calculate a firing angle that will force I_{RMS} to equal I_{ref}. The design of the current controller is discussed in more detail in section 4.4.

It is important that the 36 thyristor firings per ac cycle are equidistant, even in the presence of ac voltage distortion, because irregular firings are a source of harmonics in the ac current. Therefore, the generation of firing pulses for the main convertor and reinjection bridge are integrated into a single unit so that all the firing pulses are equidistant and synchronised, with the ac voltages in accordance with the firing angle command. Identical phase lock loops (PLL), located in each 6-pulse Graetz bridge model, are used to provide a distortion free representation of the actual ac voltage, and directly define the timing of the thyristor firing pulses in the main convertor. These pulses are passed through a dynamic delay unit, controlled by the firing angle, and the output is used to derive the pulses for the reinjection bridge. In overview, equidistant firing is assured (Ainsworth, 1968; Manitoba HVDC, 1988).

4.4 The current controller

Feedback control loops modify the dynamic performance of the compensator, therefore the controller design needs to be adequate to illustrate the compensators capabilities without diverging the discussion into a search for the perfect controller design.

The control design procedure requires each component of the current control loop to be described mathematically. One of the first attempts at characterising the ac/dc convertor was by Parrish *et al.* (1967) using a representation that is large signal and continuous. For improved accuracy, combinations of small and large signal, continuous and discrete representations have been considered in studies such as Hazell *et al.* (1970a and 1970b), Sucena-Paiva *et al.* (1973) and Millan *et al.* (1974).

As shown in later sections the large signal linear continuous model gives adequate accuracy to illustrate the dynamic capabilities of the proposed scheme and is the basis to the current controller design. This is assuming that large fast changes in firing angle are avoided and nonlinearities of the convertor are not excited, as discussed in section 4.4.3.2. Moreover, this allows the use of linear feedback control theory to determine the controller parameters and is discussed in the following sections.

A block diagram illustrating all the significant transfer functions in the compensator's control structure is shown in figure 4-9. It is assumed that the PLL and pulse generation blocks in figure 4-8 are ideal, giving perfect firing signals, and are included into the NC-SVC block. Moreover, distortion on the ac voltage is not transferred to the dc voltage and the firing angle is the only parameter controlling the ac and dc current levels. In other words, the ac system impedance is not part of the current control loop, which is a valid simplification until high ac impedances occur (such as with low frequency resonances) (Romegialli *et al.*, 1981).

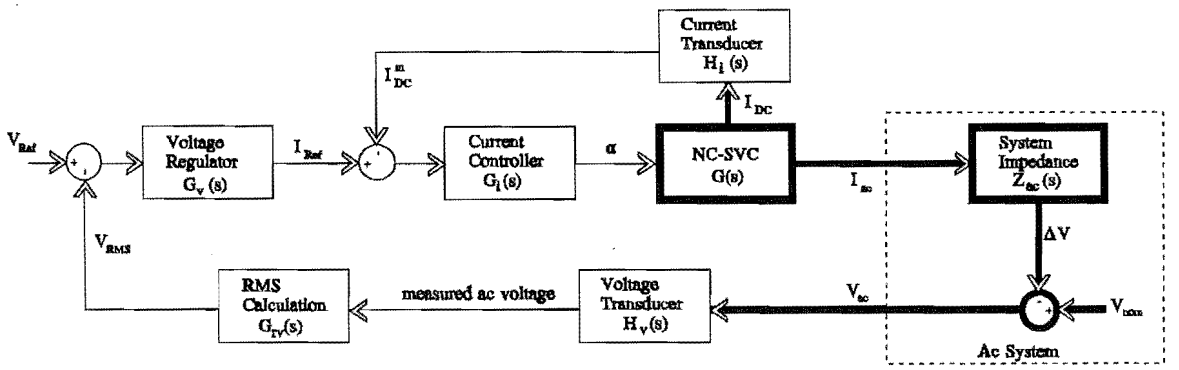

Figure 4-9: Linearised dc current feedback control loop.

The figure shows that the control structure is simplified to a nested two loop scheme. The current control loop has a significantly smaller time constant than the voltage control loop and the voltage control loop is neglected when considering the control stability of the current control loop.

4.4.1 Open loop transfer function of the current control loop

The function blocks in the current control loop consist of the NC-SVC (G(s)), dc current transducer ($H_i(s)$) and current controller ($G_i(s)$), as shown in figure 4-9. These large signal s-domain transfer functions are specified in terms of poles and zeros such that the open loop transfer function (OLTF) is

$$OLTF = G_i(s)\ G(s)\ H_i(s) = K \frac{\prod (s+a_i)}{\prod (s+b_j)} \qquad (4\text{-}2)$$

where K is the loop gain, a_i represents the i zeros and b_j represents the j poles.
For the current transducer a single pole response is typical (an example is Lisser *et al.*, 1985).

In other words, the measured current (I_{DC}^{m}) is given by

$$I_{DC}^{m} = \frac{I_{DC}}{1+sT_m} \tag{4-3}$$

where T_m is the transducer time constant.
With the NC-SVC there are two mechanisms to consider: the level of dc voltage because of the firing angle setting, and the dc current generated when that voltage is applied to the dc impedance. Assuming that the compensator remains in the single commutation mode, the average steady state dc voltage of the convertor is given by

$$V_{DC} = \frac{6\sqrt{2}}{\pi}V_1 \cos(\alpha) - I_{DC}K_eX_{MC} \tag{4-4}$$

(Kimbark, 1971). When V_{DC}, α and I_{DC} are time varying quantities, it is assumed that equation (4-4) still holds true. That is, as long as the frequency of these quantities is significantly lower than the convertor switching frequency. The switching in the convertor, however, causes a response delay with an average value of T/2 (where T is the convertor switching interval) and is represented in the voltage expression as a first order lag (Parrish *et al.*, 1967). It is assumed that the firing angle remains near 90° and $\cos(\alpha(t))$ is approximately equal to $\pi/2 - \alpha(t)$, which is defined as $\xi(t)$, therefore the s-domain expression for dc voltage is

$$V_{DC}(s) = \mathcal{L}(V_{DC}(t)) = \left[\frac{6\sqrt{2}}{\pi}V_1\,\xi(s) - I_{DC}(s)K_eX_{MC}\right]\frac{1}{s\frac{T_{SH}}{2}+1} \tag{4-5}$$

All resistances and reactances inherent in the compensator are lumped into a resistance (R) and reactance (L_{DC}) on the dc side. The application of the dc voltage to this impedance results in a dc current of

$$I_{DC}(s) = \frac{V_{DC}(s)}{(R + sL_{DC})} = \frac{\left(\frac{6\sqrt{2}}{\pi}V_1\xi(s) - K_eX_{MC}I_{DC}(s)\right)}{(R + sL_{DC})\left(1 + s\frac{T_{SH}}{2}\right)} \tag{4-6}$$

The explicit form of equation (4-6) in terms of I_{DC} has a second order denominator with

unknown roots. By approximating the denominator's first order coefficient from $L_{DC}+\frac{T_{SH}}{2}R$ to $L_{DC}+\frac{T_{SH}}{2}(R+K_eX_{MC})$, the roots become known. This approximation is possible only when L_{DC} is significantly larger than $\frac{T_{SH}}{2}R$ and $\frac{T_{SH}}{2}K_eX_{MC}$. The explicit form of equation (4-6) is

$$I_{DC}(s) \approx \frac{\frac{2}{L_{DC}T_{SH}}\frac{6\sqrt{2}}{\pi}V_1\,\xi(s)}{\left(s+\frac{(R+K_eX_{MC})}{L_{DC}}\right)\left(s+\frac{2}{T_{SH}}\right)} \qquad \textbf{(4-7)}$$

For the current controller a small steady state error is achieved with a conventional proportional-integral control structure (with an integral time constant of T_i and total gain of K). Additional lead/lag compensation is available to give improved dynamic performance. To perform the dc current controller design, discussed in the following section, an open loop transfer function is needed, which in this case is

$$OLTF=\frac{I^m_{DC}(s)}{\xi(s)} = \frac{K\,\frac{2}{L_{DC}T_{SH}}\frac{6\sqrt{2}}{\pi}V_1}{\left(s+\frac{(R+K_eX_{MC})}{L_{DC}}\right)\left(s+\frac{2}{T_{SH}}\right)}\left(\frac{\frac{1}{T_m}}{s+\frac{1}{T_m}}\right)\left(\frac{s+\frac{1}{T_i}}{s}\right)\prod\frac{s+a_i}{s+b_j} \qquad \textbf{(4-8)}$$

where a_i represents the i zeros and b_j the j poles for the lead/lag compensation.

4.4.2 Controller coefficients

The parameters in the open loop transfer function (equation (4-8)) that are defined by the compensator implementation (described in section 4.2) are shown in table 4-1. The parameters X_{MC} and R are influenced by the ac system impedance, which varies depending on the state of that system. This variability is represented by Δ.

With reference to table 4-1, it is observed that $\frac{R+K_eX_{MC}}{L_{DC}}$ is significantly smaller than the other poles in equation (4-8), potentially limiting the control loop dynamic response. Selection of $\frac{1}{T_i}$ to equal $\frac{R+K_eX_{MC}}{L_{DC}}$ causes pole cancellation, where this relies on Δ being negligible.

Similarly, $\frac{1}{T_m}$ also has a small value and it is effectively increased in value by adding lead compensation in the controller (i.e. a_1=1000 and b_1=3000).

The gain for the current controller is chosen to give the best possible dynamic performance of the current control loop, while at the same time, guaranteeing that control stability is maintained in all conditions. The root locus (Nagrath *et al.*,1986), shown in figure 4-10, illustrates the change in closed loop poles as the controller gain is increased. The poles

Component	Value
$X_{MC} = X_T + X_s$	$1.25 + 0.3 \pm \Delta$ Ω
R	$0.45 \pm \Delta$ Ω
L_{DC}	0.1 H
V_1	25 kV
T_{SH}	0.55 ms
T_m	1 ms

Table 4-1: Current control loop parameters

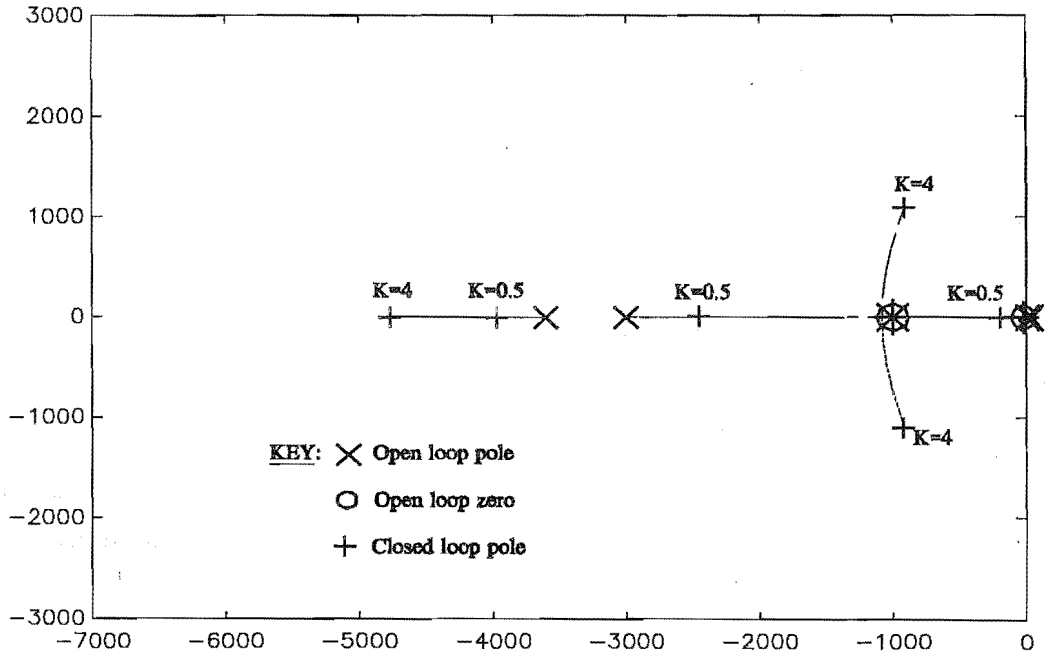

Figure 4-10: Root locus of the current controller

starting at s=0,-3000 move together on the real axis, then become complex in value. Stability is compromised when the complex poles cross the vertical axis at ω=3285 rad/s.

4.4.3 Step response of the current control loop

To confirm the theoretical dynamic response of the compensator, the software model is tested with two current controller gain settings (K). These gain settings are 0.5 and 4, chosen because they give overdamped and critically damped responses, respectively. To isolate the current controller response from the total, the voltage controller is removed from the control structure and the current reference signal is provided from a function generator, as indicated in figure 4-8. Moreover, ideal ac system conditions are maintained by representing the ac system as a voltage source in series with an inductive ac impedance. Less ideal ac system conditions are considered in chapter 5.

In the two tests, the step response of the current control loop is illustrated by forcing the current reference signal to undergo a step increase as well as a step decrease. The difference in these two responses is an illustration of the nonlinear characteristics of the ac/dc conversion in the compensator.

4.4.3.1 Overdamped response

When the controller gain is 0.5 there is one dominant pole, which is located at S=-121, giving the current control loop a time constant of 8.3 ms. In other words, the response of the theoretical control design to a step change in current command has no overshoot or oscillation, as shown in figure 4-11. The response given by the software model, shown in the same figure, contains the same trends as the theoretical, but the nonlinearity of the convertor within the compensator is also evident. The software model's response time (i.e. time to reach the 90% level) to the step increase in current command is approximately 3 ms, compared to approximately 8 ms for the control design response, whereas for step decrease the software model's response time is 12 ms.

The linear representation of the ac/dc convertor used in the controller design assumes the control delay between firing angle and dc voltage is equal to half the steady state switching interval. In this overdamped test, where the effects of the nonlinear operation are minor, the delay is decreased for the current step up and increased for the current step down. The average of the step up and step down delays is approximately the steady state value.

Finally, after the step change, the software model response also contains an oscillation with

frequency of approximately 1900 rad/s and a peak to peak amplitude of approximately 0.01 pu. Its amplitude is insignificant compared to the magnitude of the step change and is ignored because it does not effect the control stability.

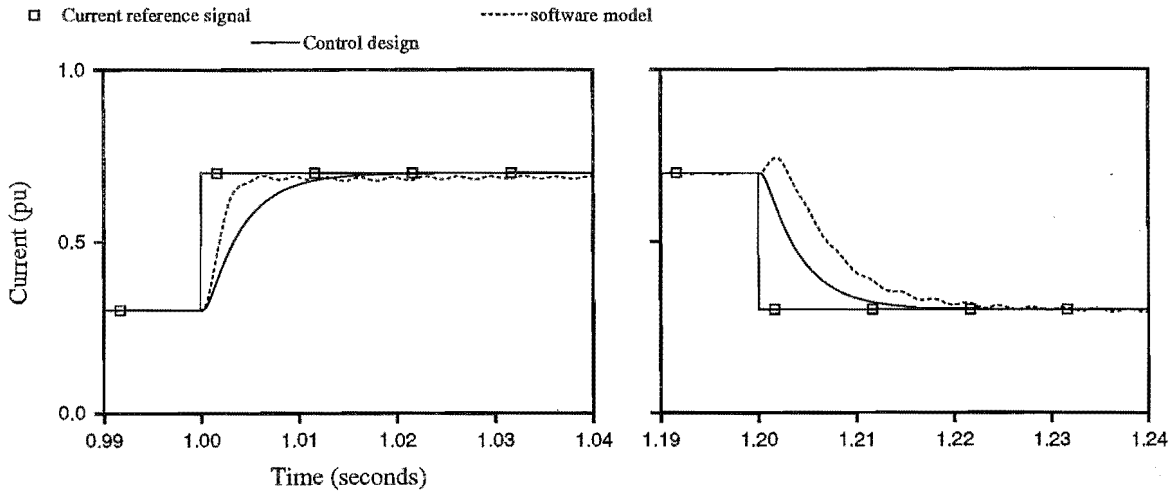

Figure 4-11: Response of the software model compared to the linear control design

4.4.3.2 Critically damped response

In the linear control design a gain of K=4 produces two dominant complex poles, as shown in figure 4-10, theoretically giving the current control loop a second order critically damped response. For comparison, the step increase and decrease responses for the software model, are shown in figure 4-12 and 4-13, respectively.

For the step increase in current reference signal (shown in figure 4-12(a) at 1.0 seconds) the controller immediately responds by forcing the firing angle to zero degrees (figure 4-12(e)) and the thyristor firing pulses are advanced in time. Immediately, maximum dc voltage is produced and the dc current increases at maximum rate (figure 4-12(a)). After approximately 1 ms, the firing angle begins to return to 90°, but the natural commutation characteristic of the convertor delays the decrease in dc voltage by approximately ¼ of a fundamental cycle. During this uncontrolled interval the dc current reaches the new current reference level (2.3 ms after the step change) and continues to rise (figure 4-12(a)). The firing angle moves toward 180°, which further delays the thyristor firing pulses by another ¼ of a fundamental cycle. Control of the convertor is regained once the dc current decreases back to the reference signal level, but the reinjection scheme is malfunctioning and correct operation is not regained

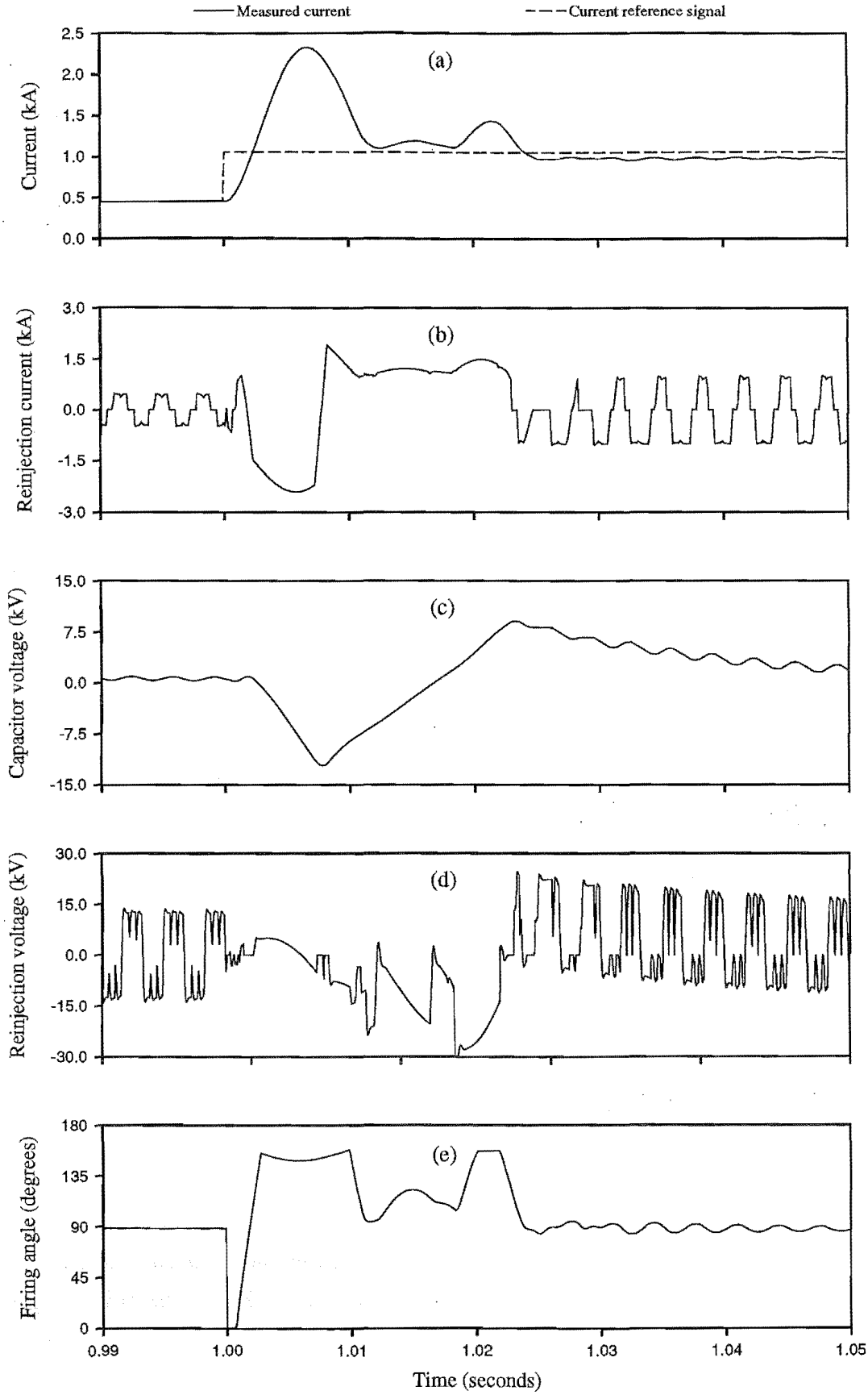

Figure 4-12: Step change in operating point

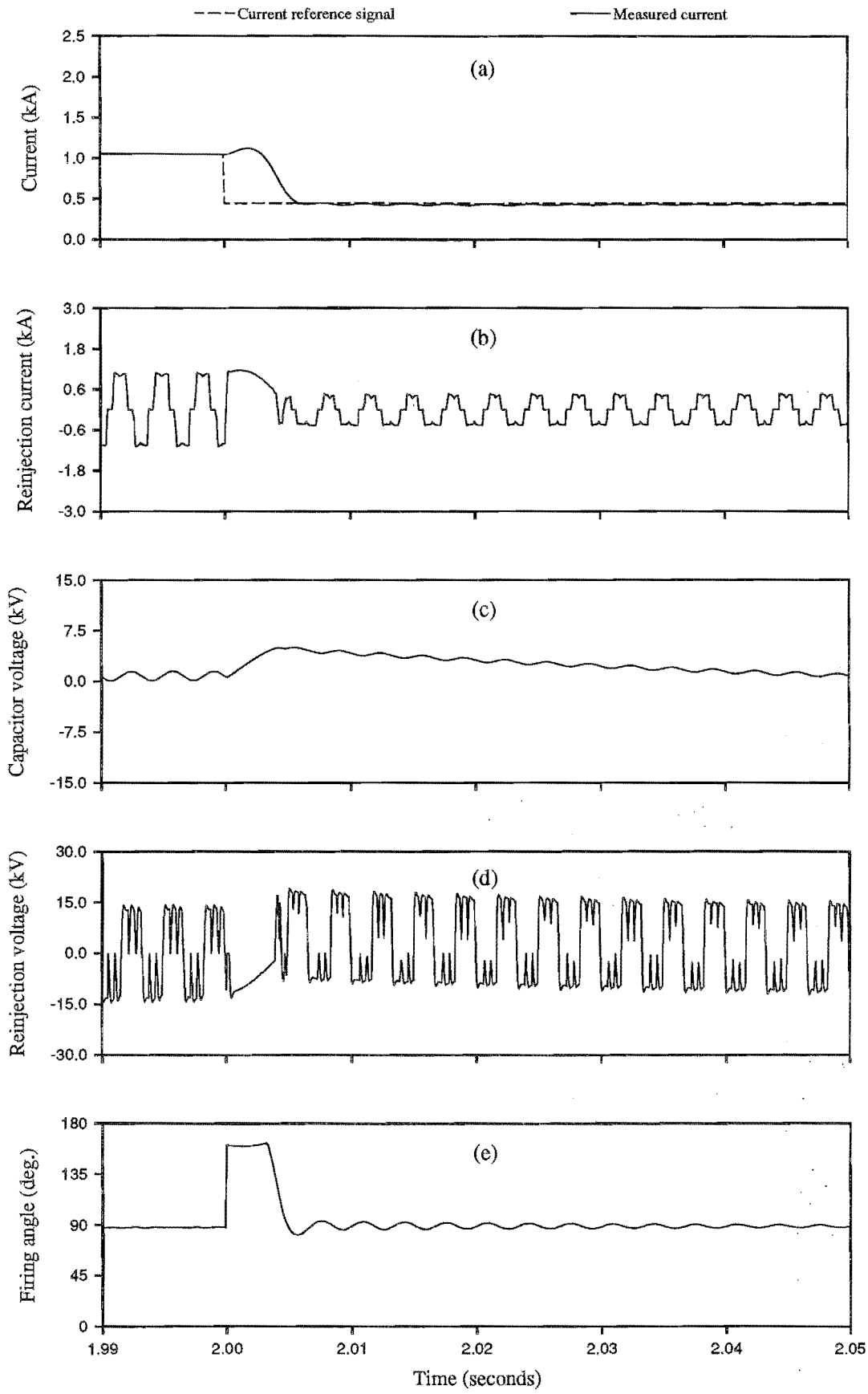

Figure 4-13: Step decrease in current level

until approximately 30 ms after the step change.

When the firing angle changes from 0° to 180° the delays in thyristor firings and change in dc current cause the reinjection current to become asymmetrical (figure 4-12(b)). This current flows through the blocking capacitors generating significant capacitor voltage excursions (figure 4-12(c)). The relative polarity of the voltages across the two blocking capacitors are such that they add to the reinjection voltage, and the reinjection voltage acquires a dc offset. Moreover, the main convertor waveshapes are distorted and the reinjection voltage is unipolar (figure 4-12(d)), therefore the reinjection bridge can no long commutate. Malfunction lasts until the dc offset in the reinjection voltage has decayed sufficiently for the reinjection bridge to commutate once more.

With the step decrease in current reference signal (shown in figure 4-13(a) at 2.0 seconds), the firing angle immediately increases to maximum (figure 4-12(e)), i.e. approximately 180° minus the safety margin to prevent commutation failure. The thyristor firings are delayed and it is approximately ¼ of a fundamental cycle before the dc voltage reaches the maximum negative value, at which time the dc current reduces at maximum rate (figure 4-12(a)). When the measured current approaches the current reference signal, the firing angle moves toward 90°. There is no response delay between the change in firing angle and dc voltage and the measured dc current settles to the current reference signal at approximately 2.006 ms.

As in the step increase case, the reinjection current is asymmetrical immediately after the step change (figure 4-12(b)) and the blocking capacitor voltage is offset along with the reinjection voltage (figure 4-12(c) and (d)). In this case, however, changes in firing angle are significantly less, the reinjection voltage remains bipolar and the reinjection scheme remains operational throughout.

In overview, when the controller gain is increased, the compensator nonlinearity causes it to malfunction before instability occurs, as described by the linear control theory. As shown in the step responses, a sudden difference in measured and reference current cause large sudden changes in firing angle (in the order of ±90°). It is the resulting deviations from the average switching interval that constitute the nonlinearity. Depending on the polarity of the change, the thyristor pulses are either advanced so that maximum positive dc voltage is immediately applied, or the thyristors are delayed to give maximum negative dc voltage. Either way, this response (to achieve maximum voltage) is independent of convertor pulse number. In other words, a 6-pulse convertor responds the same way as a 36-pulse version.

For the nonlinear behaviour of the NC-SVC to be permissable in normal operation, then a better controller is needed. For example, a controller that uses a nonlinear algorithm to restrain the changes in firing angle so that the measured current does not overshoot when the uncontrolled period of operation is imposed. Moreover, by detecting sudden large changes in firing angle the reinjection scheme and parts of the current controller can be bypassed before

another action and malfunction is avoided.

All waveforms in figure 4-12 and 4-13 appear to reach a new steady state condition within approximately 40 ms, but this is not the case for the capacitor voltage. The component of this voltage that adds to the reinjection voltage decays within 40 ms, but the changes in main convertor dc voltage excite the LC resonance that exists between the blocking capacitor and magnetising inductance of the reinjection transformer. The capacitor voltage from figure 4-12 is redrawn in figure 4-14 with a longer timebase, revealing an oscillation of approximately 2 Hz.

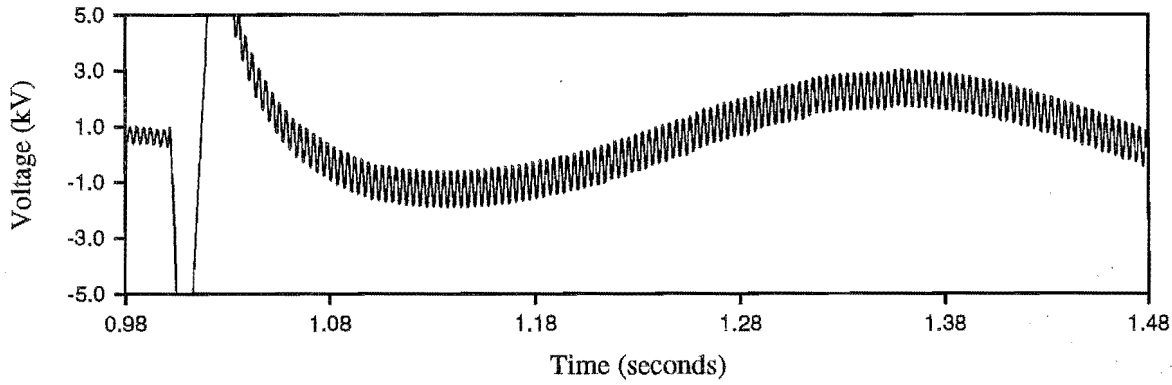

Figure 4-14: Capacitor voltage during the low frequency resonance

The model is implemented with a linear magnetising inductance in the reinjection transformer, causing the single low frequency oscillation on the blocking capacitor voltages. The relative polarity of these voltages is opposite to that occurring for the 6^{th} harmonic voltages, generated by the reinjection current. In the latter case, 6^{th} harmonic voltage is added to the reinjection voltage, as indicated by equation (3-7). The low frequency oscillating voltage, however, is not added and there is no influence on the reinjection scheme operation. The presence of saturation in the reinjection transformer potentially eliminates single frequency oscillations, damping the oscillation. On the other hand, it is possible that chaotic behaviour will occur (Araujo *et al.*, 1993), with potentially destructive effects.

4.5 Dynamic performance

In the last section the dynamic tests of the software model focus on the control stability of the current controller in ideal ac system conditions. In this section, the tests are expanded to include the voltage control loop and an ac system environment that has inherent variation in the ac voltage magnitude.

This system environment, shown in figure 4-15, consists of a Thevenin equivalent circuit, i.e. a voltage source (E) in series with an impedance (Z_S), representing the utility supply. The Thevenin simplification is valid up to approximately 0.5 seconds after the occurrence of a

disturbance, since other controlling mechanisms in the system, such as generator governors and taps in transformers, do not respond immediately (Miller, 1982; Ainsworth *et al.*, 1980). Moreover, an adjustable impedance type load is included that causes variation in the bus voltage magnitude. The SVC is also connected directly to the ac bus. It consists of a 100 MVAr absorption component, either the TCR or NC-SVC, and a 90 MVAr fixed capacitor bank, forming a SVC capable of compensating for the reactive power variations of the load, and hence is able to control the bus voltage.

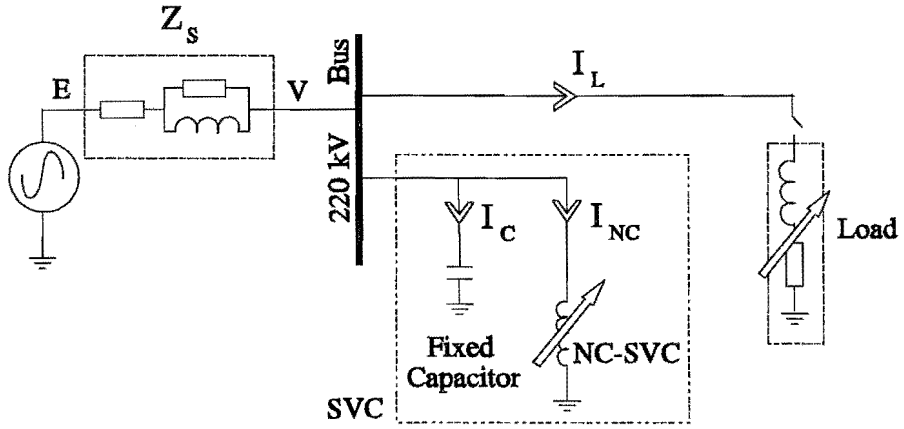

Figure 4-15: Test system.

By varying the impedance of the ac load, to provide a balanced disturbance in the ac system, the compensator's response is shown in figure 4-16. At 0.7 seconds the load circuit breaker is opened, causing the bus voltage (V) to quickly rise (see figures 4-16(b) and 4-16(a)). Without the compensator, the bus voltage settles to a steady value of 1.056 pu. With the compensator, the increase in voltage is detected causing the NC-SVC to increase its ac current level (I_{NC}), as shown in figure 4-16(c), and within 50 ms the voltage is restrained to a level defined by the controller slope (figure 4-7). Note that the load rejection excites a resonance between the fixed capacitor and supply inductance, disturbing both the bus voltage and capacitor current (I_C) waveforms (figures 4-16(a) and 4-16(d)). The effect of the resonance on the NC-SVC operation, however, is negligible. Ac voltage distortion is discussed further in chapter 5.

One of the expected benefits of the NC-SVC is a fast response capability because of the large number of controllable switchings per cycle. However, the oscillograms in figure 4-16 show that the NC-SVC has a time constant in the order of 50 ms. This is attributed to the AVR, which slows the response of the NC-SVC considerably. To demonstrate the NC-SVC's fast response capability the AVR is replaced with a waveform generator that injected a test signal into the dc current reference, as indicated in figure 4-8. Sinusoidal and square wave dc current

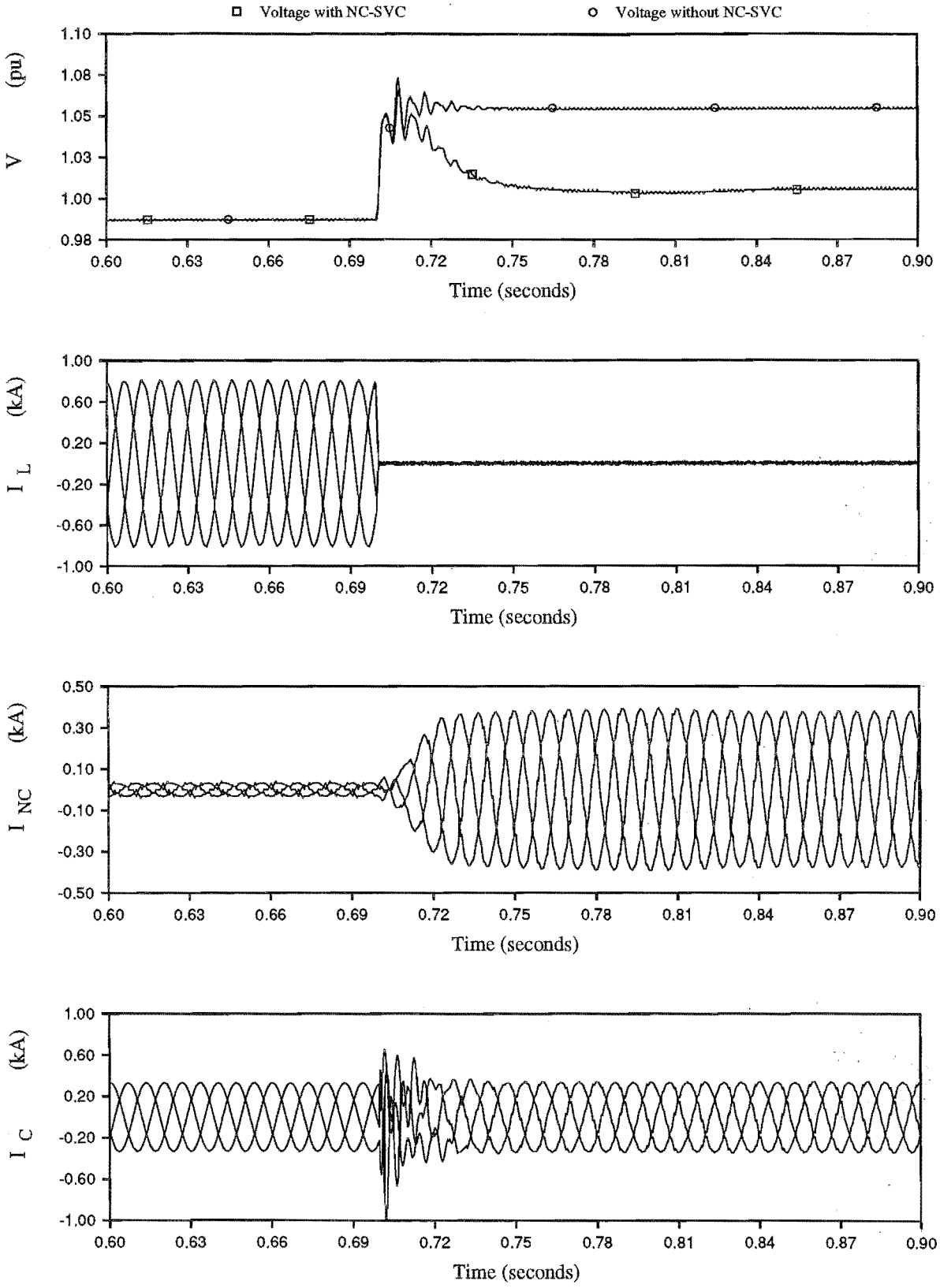

Figure 4-16: Oscillograms of a large change in load

reference signals were used to oscillate the dc current between 0.25 kA and 1.25 kA at 10 Hz, as shown in figures 4-17 and 4-18. In both simulations the dc current reference trace and measured dc current are superimposed onto the same oscillogram to emphasise the response of the current control loop.

The results from the sinusoidal reference simulation show that the dc current control loop is able to track the demand signal with a gain of 0.95 and delay of 2.4 ms. The square wave reference simulation shows that the NC-SVC responds to the step change in dc current reference in approximately 1 ms, but there is a limit to the rate of change in dc current because of the dc impedance value and maximum dc voltage available. It takes approximately 5 ms to reach the new dc current reference. To increase the maximum rate of change of dc current above 250 A/ms, measured from figure 4-17, the time constant of the dc impedance must be decreased. This must be matched with a decrease in dc current control time constant to prevent an ac system disturbance from moving the NC-SVC's operating point away from the required level.

The nonlinearity observed in figures 4-11, 4-12 and 4-13 are not significant in figure 4-17. This is attributed to the choice of controller gain (giving an overdamped response), as well as the current reference signal being filtered to reduce the rate of change of firing angle. During the single commutation mode, compensator current is proportional to the dc current. This is illustrated with oscillograms in figures 4-17 and 4-18 confirming that by controlling the dc current, there is direct control over the ac current amplitude with minimal delay, and that the ac current does not experience any uncontrolled oscillations.

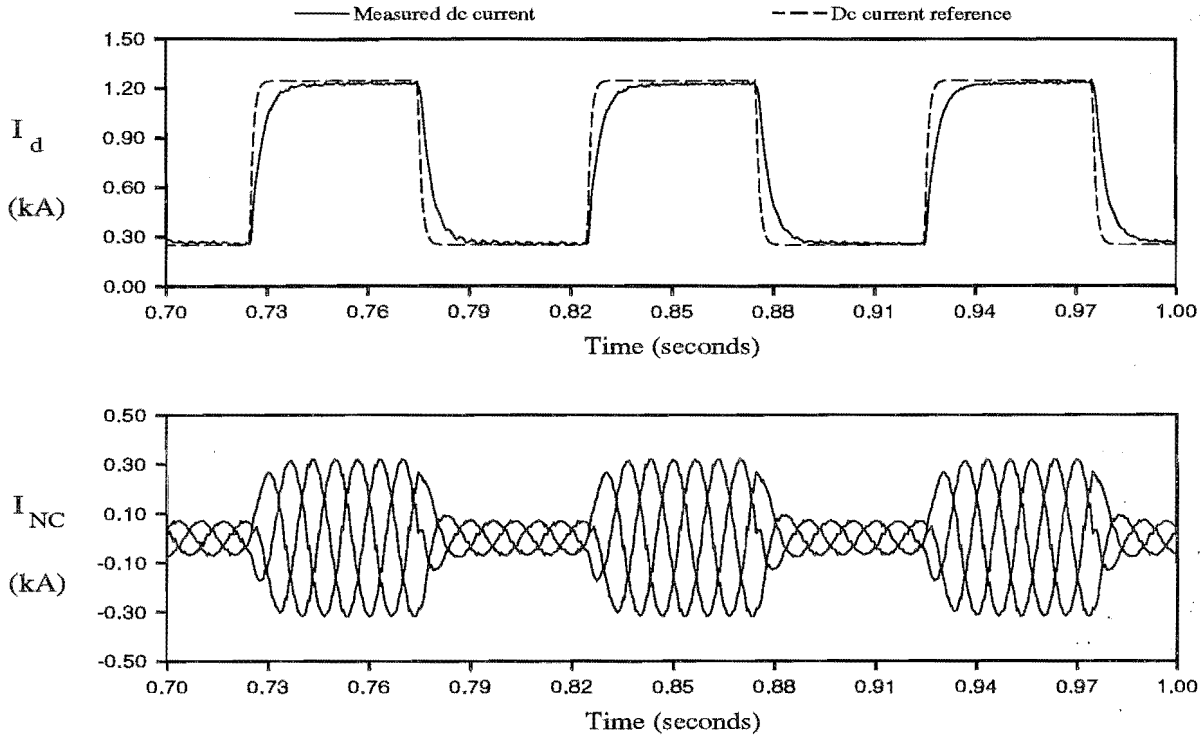

Figure 4-17: Current controller response to a Square wave current reference signal.

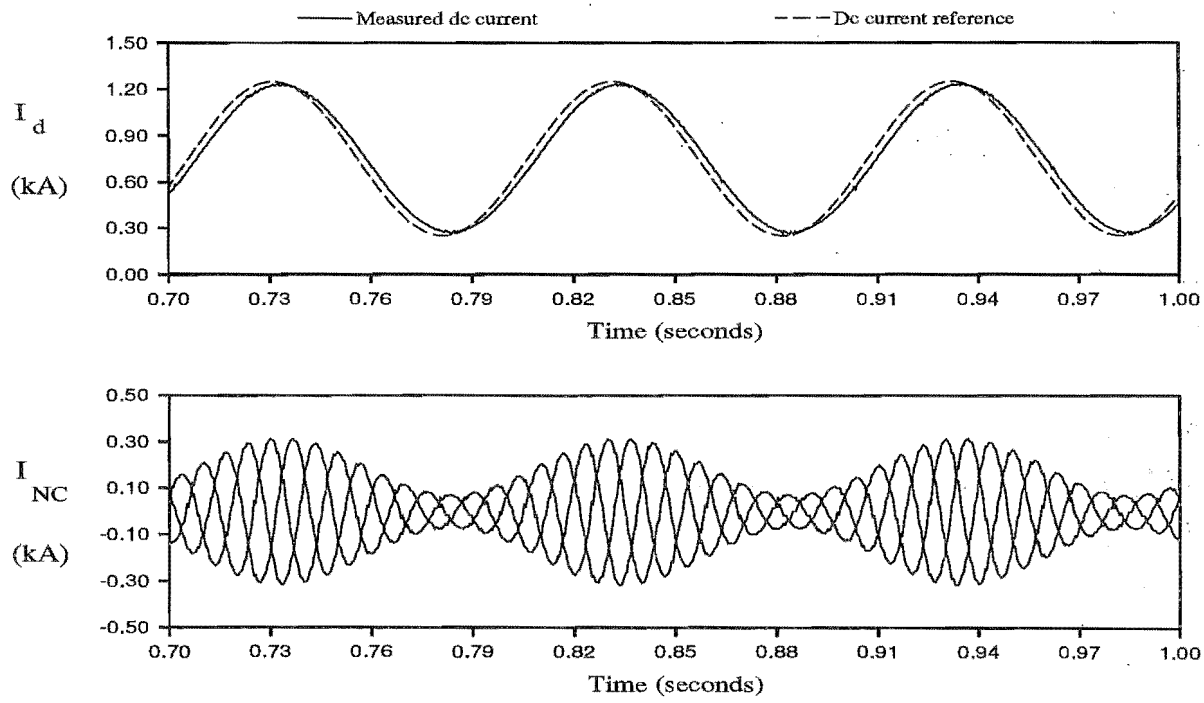

Figure 4-18: Current control loop response to a sinusoidal current reference signal.

4.6 Conclusion

In this chapter a software model of the proposed compensator, which is implemented into the EMTDC-PSCAD simulation package, is described. Simulated steady state current and voltage waveforms from the 100 MVAr software model reaffirm the predicted compensator operation. The duration of the reinjection bridge commutations agree with the predicted values (chapter 3) only when the blocking capacitor value is large. The blocking capacitor value, defined by the criteria in chapter 2, significantly reduces the commutation interval.

The change in compensator current, i.e. fundamental and harmonic content, over the firing angle range defining the single commutation mode (82° to 90°), is consistent with the theoretical values given in chapter 2. Resistance in the circuit effectively stretches this characteristic over a larger firing angle range. Once commutation overlap occurs below 82° firing angle, the reinjection scheme stops operating correctly and there is a sudden increase in compensator current harmonics.

The compensator controller is an important factor in the compensator dynamic response and a nested three loop linear control structure is described in preparation for the dynamic studies in chapter 5. The linear representation of the ac/dc conversion process is reasonable approximation in the control design, as long as large sudden changes in firing angle are avoided. Extreme changes in firing angle cause the reinjection scheme to malfunction and low pulse operation occurs.

Simulating an ac load rejection in a simplified power system representation shows that the NC-SVC is able to regulate the ac voltage, but with a slow response dictated by the voltage controller. Faster changes in compensator current caused by the injection of an auxiliary signal into the controller show that NC-SVC begins to respond to changes after approximately 2 milliseconds, but dc impedance limits the rate of change of current. For all of these dynamic simulations, the compensator current does not exhibit any uncontrolled oscillations. Furthermore, the overdamped response experienced by the hardware model is not present, thus the computer model has the advantage of providing an insight into both the steady state and the dynamic performance of the NC-SVC.

Chapter 5

Power system aspects

In the previous chapters the focus of the discussion is the characteristics and internal operation of the compensator. In this chapter the perspective is changed to the compensator being a component in the power system and is tested in that context. From the ac power system's perspective, an ideal compensator provides the desired level of reactive current for each phase with no distortion, independent of the ac system conditions. In reality, ac voltage unbalance and distortion modifies the compensator operation and the resulting compensator current distortion and unbalance in turn disturbs the ac system.

The software model of the compensator, described in chapter 4, provides the means to test the system-compensator interaction within the EMTDC-PSCAD simulation package. A variety of ac system conditions are considered in this chapter, including steady state with and without voltage distortion to gauge acceptability of the compensator current harmonics. In addition, dynamic operation resulting from ac system disturbances is considered to determine the compensators speed of response and the conditions that cause malfunction. A 12-pulse thyristor controlled reactor (TCR) is also modelled and operated in the same ac system conditions. This enables the TCR to be compared with the NC-SVC, thus providing a relative measure of the NC-SVC's performance with respect to a commonly constructed and well known topology.

5.1 Compliance with harmonic standards

There are a many different harmonic standards or recommended practices describing acceptable levels of harmonic injection (Heydt, 1991). Variations between standards,

combined with the complexities of the ac system configuration makes it impossible to give a general answer to the acceptability of the compensator harmonics, the conditions for each installation must be taken into account. To give an indication of the acceptability of the compensator's harmonic current levels, two standards are chosen: IEEE recommended practice (IEEE std-519, 1992) and the Electrical supply regulations of New Zealand (NZECP-36, 1993). Both standards specify the allowable harmonic currents and voltages at the point of common coupling and propose ways of estimating the likelihood of telecommunication interference.

The compensator current harmonic content, derived with the help of the software model operating at rated current, is shown in table 5-1. Theoretical harmonic values are also included, where the effects of the commutation process are included, assuming the duration of all commutations is 2.6°, which is the theoretical commutation interval at rated current, as defined by equation (3-15). From IEEE std-519, telephone influence factor (TIF) weightings (w) for each harmonic are interpolated from the 60 Hz values to 50 Hz equivalents and included in the table. The Current/TIF product (I.T.) is calculated at 82631, which is in category III of possible interferences, i.e. the harmonic currents are at "Levels that probably will cause interference". A survey of how much each harmonic contributes to the I.T. values shows that the 36±1 harmonics are dominant.

The harmonic current limits from both standards are also shown in the table, whereby the suggested modifications to the IEEE std-519 limits, if high pulse convertors are involved, is ignored. These standards differ in that the values from NZECP-36 are fixed maxima for a

Harmonic number (h)	Harmonic current (amperes) (I_1=262 A, μ_R=2.6°) Measured(I_h)	Theory	TIF weighting (w) IEEE-519	I_h x w	Harmonic Current limit (amperes) (I_1=262 A) NZECP-36	IEEE std-519
11	2.09	1.14	1398	2921	1.6	2.62
13	1.62	1.04	2185	3540	1.4	2.62
23	1.68	0.55	5665	9517	0.8	0.79
25	1.39	0.50	6015	8360	0.7	0.79
35	7.88	6.69	7362	58013	0.7	0.39
37	7.09	6.25	7778	55146	0.7	0.39
47	1.17	0.26	9882	11562	0.7	0.39
49	1.00	0.18	10298	10298	0.7	0.39
	THD=4.29%	THD=3.56%		I.T=82631		THD=2.5%

Table 5-1: Harmonic current magnitudes

given system voltage and IEEE std-519 values are dependent on the fundamental current rating of the compensator. Comparison of the measured and theoretical harmonics with the specified limits show that only the theoretical harmonics conform to NZECP-36, except for the 36±1 harmonics. Since NZECP-36 limits are fixed for a given ac voltage, the measured compensator harmonics can become more favourable if the VAr rating is reduced. For the IEEE std-519, the measured 12±1 harmonics and theoretical 12±1, 24±1 and 48±1 harmonics conform to the harmonic limits. Again, the 36±1 harmonics are significantly larger than the allowable levels, not only exceeding the individual limits, but also forcing the maximum total harmonic distortion (THD) to be exceeded (ie. THD is 4.29% compared to the 2.5% limit). When the compensator current flows into the ac system equivalent, consisting of a 220 kV voltage source in series with a 24.2 Ω reactive impedance, the ac voltage at the point of common coupling is distorted with harmonic magnitudes as shown table 5-2. The relevant voltage limits from both NZECP-36 and IEEE std-519 are also shown. NZECP-36 is significantly more stringent than IEEE std-519, causing most of the measured harmonics to fail NZECP-36, while they pass the IEEE std-519 values. The 36±1 harmonics are consistently at unacceptable levels, being approximately an order of magnitude larger than the limits. The other harmonics vary between satisfying and failing the standards, depending on whether measured or theoretical harmonic magnitudes are used and which harmonic standard is considered. Consequently, the THD of the voltage waveform is significantly larger than the

Harmonic number (h)	Harmonic voltage (%) ($V_h = 24.2hI_h$)	Voltage limit (%) NZECP-36	Voltage limit (%) IEEE std-519
11	0.44	0.7	1.0
13	0.40	0.6	1.0
23	0.74	0.3	1.0
25	0.66	0.3	1.0
35	5.25	0.3	1.0
37	5.0	0.3	1.0
47	1.05	0.3	1.0
49	0.93	0.3	1.0
	THD=7.5%		THD=1.5%

Table 5-2: Measured harmonic voltages compared to the standards

IEEE limit.

To compare the proposed compensator's harmonic performance against an existing technology, the maximum harmonic magnitudes of an equivalently rated (steady state) 12-pulse thyristor controlled reactor (TCR) is shown in table 5-3. The table shows two sets of data, depending on the TCR's overload capability. For the typical case where the overload capability is negligible, comparison with the theoretical harmonics of the NC-SVC shows that the NC-SVC has smaller 12±1 harmonic magnitudes, but significantly larger 36±1 harmonics. This comparison is biased against the NC-SVC, which has significant overload capability (approximately 4 pu, defined by the system and transformer impedance), while the typical TCR does not. When the TCR design is modified to include an equivalent overload, i.e. by reducing the impedance of the reactors, the maximum harmonic magnitudes in the rated operating region (shown in table 5-3) are significantly larger than the theoretical NC-SVC harmonics, except for the 36±1 orders.

Harmonic number		11	13	23	25	35	37	47	49
maximum I_h in rated range (amperes)	no overload	2.8	2.0	0.63	0.52	0.26	0.24	0.16	0.16
	with overload (max. I = 4 pu)	8.7	5.5	1.9	1.7	0.81	0.76	0.47	0.47

Table 5-3: Harmonic content of a 12-pulse thyristor controlled reactor.

Descriptions of actual TCR installations indicate that for the 11^{th} harmonic and above only a high pass ac filter is required (examples are Miller, 1982; Thanawala, 1985; Lowe *et al.*, 1990; Muttik *et al.*, 1991). The same principle holds for the NC-SVC, but the filter rating must be higher to eliminate the higher levels of 36±1 harmonics. An alternative to passive filters for removing the 36±1 harmonics is to increase the pulse number of the compensator further with additional components in the reinjection scheme (Villablanca, 1992). However, as mentioned in chapter 2, the pulse multiplication is only approximate and low levels of 12-pulse related harmonics are always present.

5.1.1 Very high pulse number

The level of pulse multiplication carried out by the reinjection scheme depends on the number of parallel connected reinjection bridges and their associated reinjection transformer secondary windings (Villablanca, 1992). At regular intervals the reinjection bridges are switched such that each reinjection transformer secondary winding consecutively carries the dc current, creating a multilevel reinjection current in the primary winding of the reinjection transformer.

The turns ratio between the primary (N_0 turns) and each of the K secondary windings (N_i turns, where i equals 1,2,3...K) of the reinjection transformer is

$$\frac{N_i}{N_0} = \cot\left(\frac{\theta}{2}\right) \tan\frac{\theta(K+1-i)}{(2K+1)} \qquad \textbf{(5-1)}$$

where θ is the conduction interval of the main convertor (Villablanca, 1992). The tan function is approximately linear over the region of use, showing that an increase in pulse number forces the reinjection current to take a triangular waveshape.

The effect of this reinjection current is illustrated by considering an ideal 256-pulse convertor. Because the transformer secondary current (I_{S1}, see figure 2-1) is formed by adding the reinjection current to the conventional 6-pulse waveform, I_{S1} also has a triangular waveshape, as shown in figure 5-1. The harmonic content of the secondary current is also shown in this figure, illustrating that the low order 6-pulse related harmonics remain at similar magnitudes as with the 36-pulse NC-SVC case.

The main transformer combines the two main bridge ac currents, producing the compensator current shown in figure 5-2. Ignoring the current steps in the waveshape, the trend in the resulting current waveform is not sinusoidal, but 12 segment piecewise linear, the number of segments directly relating to the pulse number of the main convertor. From the harmonic content of this waveform, shown in the same figure, the 6-pulse related harmonics are eliminated, leaving small quantities of 12-pulse related harmonics below the characteristic harmonics, in the same fashion as the 36-pulse case.

Comparing the 12-pulse related harmonics with those present in the 36-pulse compensator show that the 12±1 harmonics in the very high pulse case are larger by a factor of approximately 1.6. It can be shown that these harmonics get larger as the number of reinjection bridges increase, reaching a limiting value above 3 reinjection bridges. Reconsideration of the harmonic limits show that the theoretical harmonics levels (in figure 5-2) pass both the NZECP-36 and IEEE std-519, except for the 12±1 harmonic limits in the NZECP-36 standard. With rated current of 262 amps, figure 5-2 shows that the 11^{th} and 13^{th} harmonic magnitudes are both 1.8 amps.

5.2 Operation in the presence of ac voltage distortion and unbalance

In this section steady state ac voltage distortion and fundamental frequency unbalance are considered, whereas transient phenomena is discussed in section 5.3. In normal ac system operation, both the utility and consumer are obliged to maintain the ambient steady state voltage distortion below the levels prescribed in the harmonic standards. These levels of distortion have negligible effect on the harmonic content of the compensator current described

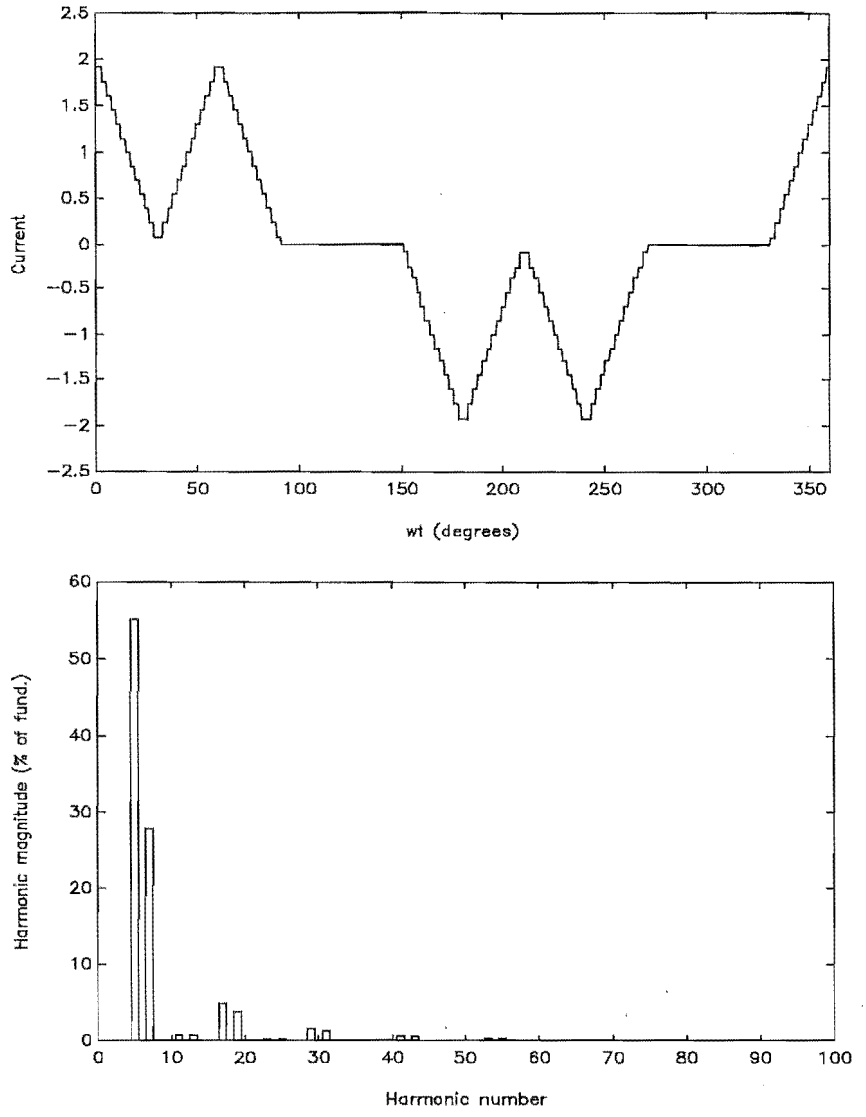

Figure 5-1: Theoretical main transformer secondary current when the pulse number is 256.

in section 5.1. There is always the possibility, however, that at least one ac system contingency results in severe voltage distortion for a finite period, which from the compensators point of view is steady state. For example, resonances are a common cause of harmonic voltage distortion potentially reaching large magnitudes. Fundamental frequency unbalance usually occur because of severely unbalanced loads, in which case the compensator is used to perform phase balancing (Hauth *et al.*, 1982), as considered in the next section.

To illustrate the compensator response to voltage distortion, it is simulated while negative sequence 5^{th} harmonic voltage is added in series with the supply voltage source. Similarly, fundamental frequency unbalance is tested by adding negative sequence fundamental voltage. This is the same technique is used by Gyugyi *et al.* (1980) to test a TCR.

In both simulation cases the added voltages are 10 kV in magnitude, i.e. 8% of positive

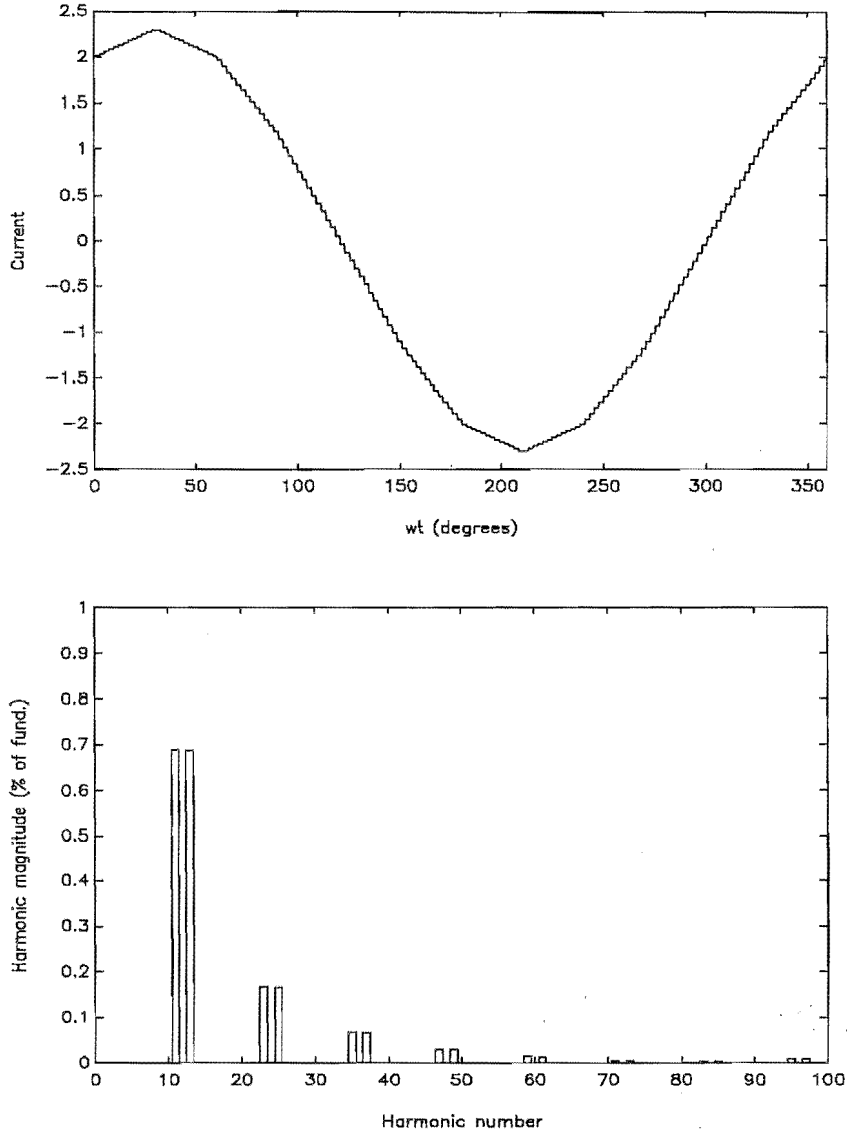

Figure 5-2: Theoretical compensator current when the pulse number is 256.

sequence fundamental. Moreover, the compensator is operated with constant firing angle, thus removing the effects of the controller. The results are compared to tests with an equivalently rated 12-pulse NC-SVC and a 12-pulse TCR; they are shown in figures 5-3 and 5-4, where the three harmonic phase current information is separated into positive and negative sequence harmonic information. Zero sequence is not shown because none of the compensators can generate zero sequence via their switching action.

Figures 5-3 and 5-4 show that the presence of voltage distortion or fundamental frequency unbalance results in all compensators producing current components of the same harmonic order and sequence. Furthermore, if the added ac voltage is defined as the k^{th} order negative sequence ac voltage, the resulting compensator current also has components of other harmonic orders. The predominant component is the $(k+1)^{th}$ positive sequence harmonic, whereby its

magnitude indicates that there is significantly more crossmodulation in the NC-SVC topologies than the TCR.

Theoretically, conventional ac/dc convertors not only produce the $(k+1)^{th}$ harmonic, but also higher harmonic orders of $(mp + 1 \pm n(k+1))$ negative sequence and $(mp - 1 \pm n(k+1))$ positive sequence, where p is the pulse number and, m and n=1,2,3,...(Wood, 1993).

For both NC-SVCs (i.e. p=12 and 36), significant levels of harmonics associated with n=1 are observed. The proposed scheme also contains low levels of harmonics corresponding to a 12-pulse response, but they are likely to be associated with compensator design uncertainty and inaccuracies in the thyristor firing (i.e. interference with the phase lock loop). The proposed scheme is sufficiently different from the 12-pulse case to assume that ideally its response is 36-pulse in nature.

In the discussion so far the compensator has operated with constant firing angle. When both the current and voltage controllers are included in the compensator, the current and voltage distortion is detected and the controller attempts to compensate. In the case with negative sequence fundamental ac voltage the current reference signal (I_{ref} as shown in figure 4-9) is measured at $0.74 + 0.57\sin(2\omega t)$ pu and the firing angle (α as shown in figure 4-9) is measured at $87.9 + 6.1\sin(2\omega t)$ degrees. As a result the negative sequence fundamental component of the compensator current increases from 2.4% (shown in figure 5-4) to 8.3% and its phase is such that the negative sequence fundamental component of the ac voltage is decreased by 3.3%.

The compensator has a similar response to 5^{th} harmonic distortion on the ac voltage. The current reference signal is measured at $0.73 + 0.0067\sin(6\omega t)$ pu and the firing angle is measured at $87.6 + 2.5\sin(6\omega t)$ degrees. The relative phase of the resulting ac current distortion and the distortion on the ac voltage is such that the voltage distortion is reduced by 2.7%.

For both the distortion and fundamental frequency unbalance cases it is shown that the controller automatically reduces their magnitude at the point of common coupling rather than aggravating it. Comparison of the ac current harmonics with and without the controller (see figures 5-3, 5-4 and 5-5) shows that the variation in firing angle (also called modulation) causes a proliferation of noncharacteristic harmonics, i.e. $35\pm nk$ (negative sequence) and $37\pm nk$ (positive sequence) harmonics, while also decreasing the magnitude of the characteristic harmonics.

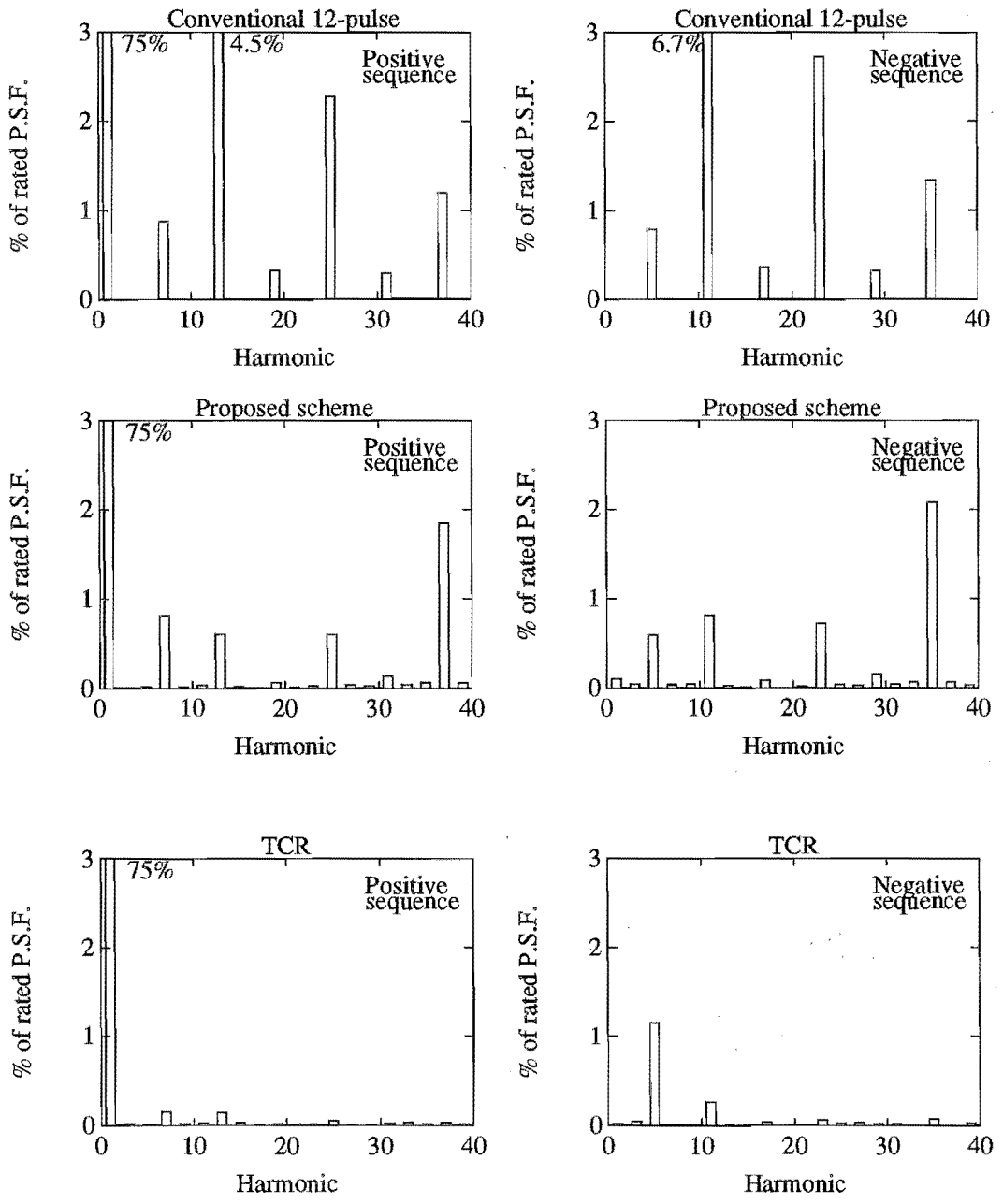

Figure 5-3: Ac current harmonics when the firing angle is constant and the ac voltage contains a 5^{th} harmonic.

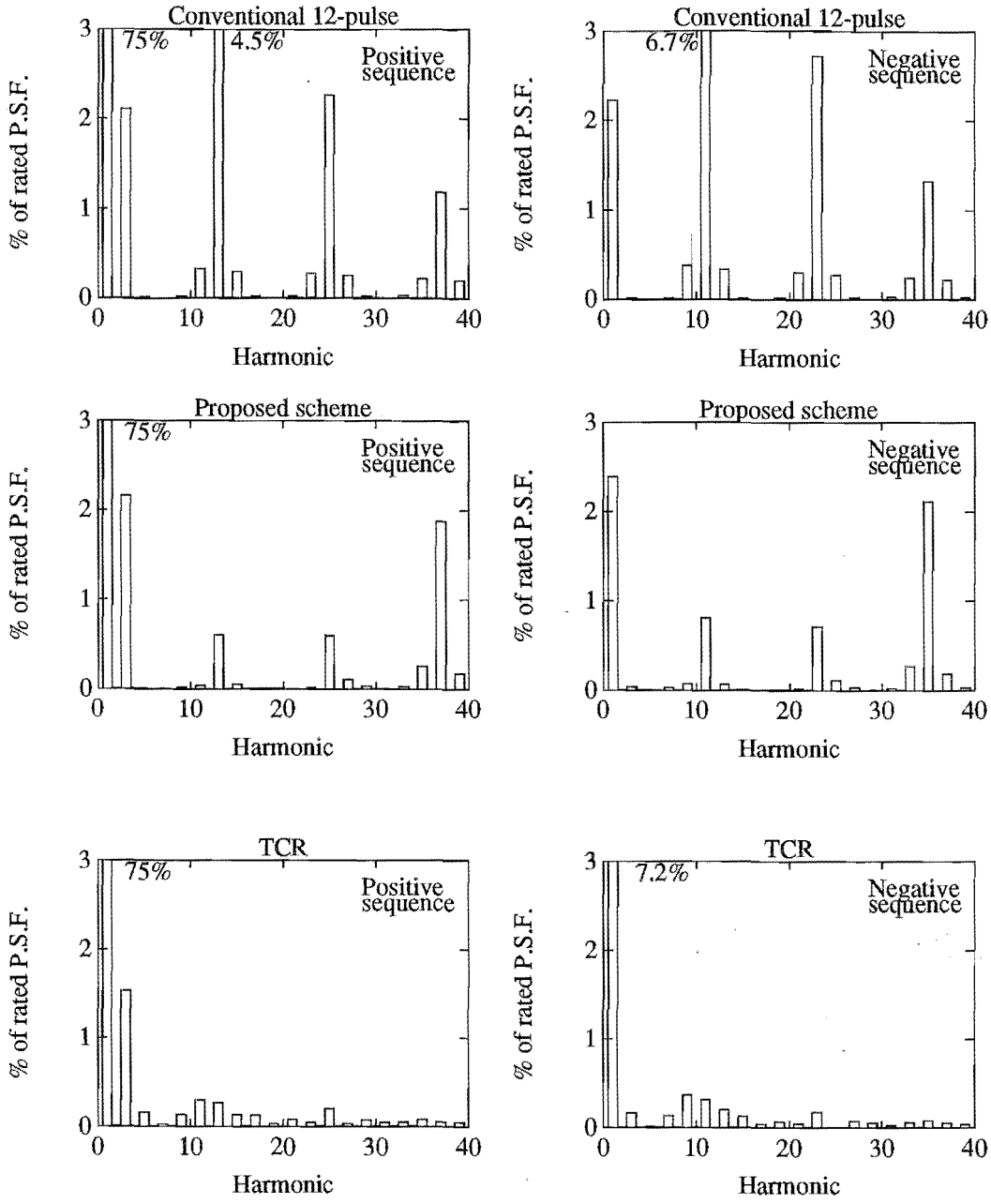

Figure 5-4: Ac current harmonics when the firing angle is constant and the ac voltage contains negative sequence fundamental.

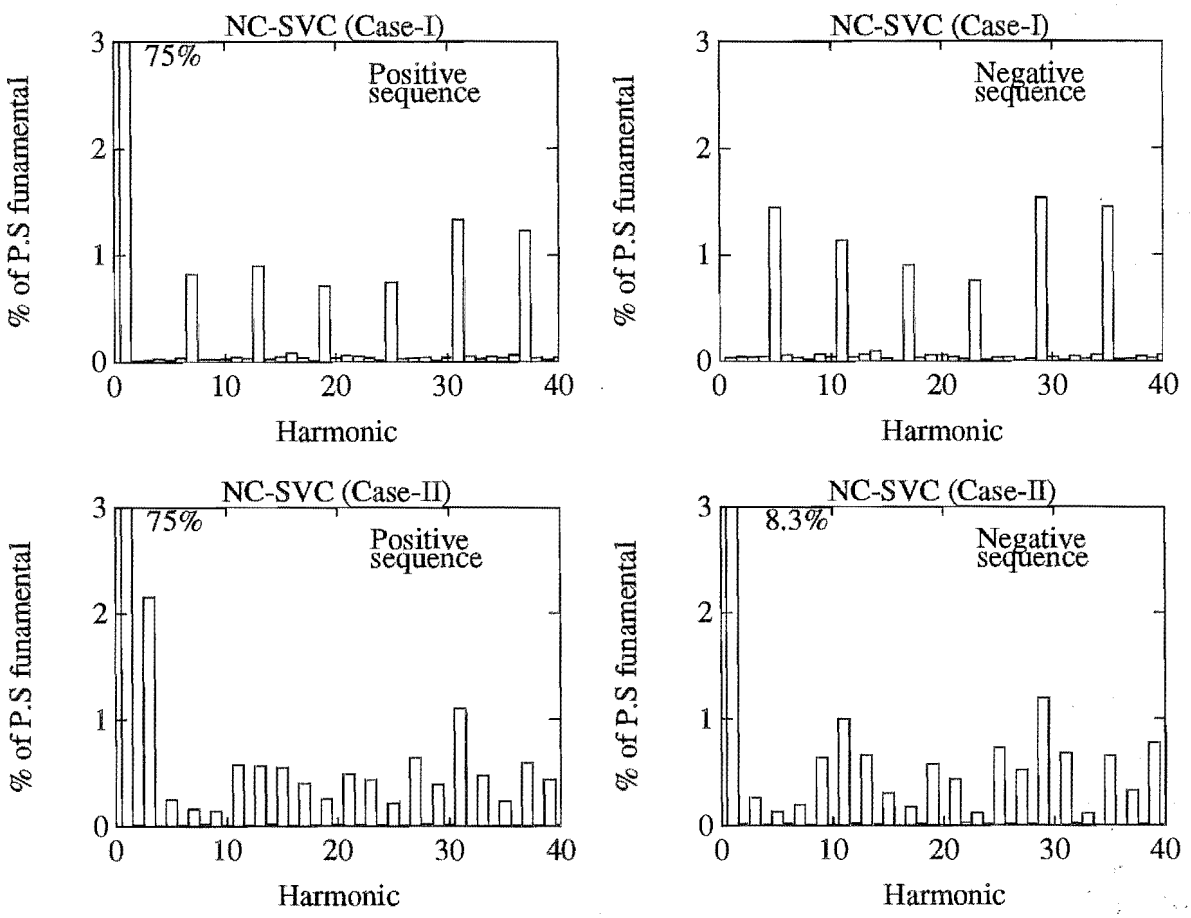

Figure 5-5: Compensator current harmonics when there is ac voltage distortion.
case-I: 5^{th} harmonic negative sequence voltage
case-II: fundamental freq. negative sequence voltage

5.2.1 Compensation of negative sequence fundamental voltage

Unbalanced loading of the three phase system is often compensated with shunt VAr components on a per phase basis to prevent the generation of zero or negative sequence fundamental in the ac voltage (Hauth *et al.*, 1982; Miller, 1982; Hanson, 1985). This is necessary because these sequences increase losses in the system, particularly in three phase rotating machines such as induction motors (Woll, 1975; Miller, 1982). With large single phase loads, such as with electric trains or mining equipment, or erratic three phase loads, such as the arc furnace (Grünberg *et al.*, 1986), that continuously vary their operating points, the VAr compensation also needs to be continuously adjustable.

The delta connected 6-pulse TCR is a common topology used for per phase VAr compensation (i.e. individual phase control), because it is constructed from three single phase devices that can be independently controlled to produce positive and negative sequence fundamental in the compensator current (Hanson, 1985; Lowe, 1989). This is at the expense of producing all orders of odd harmonics in the compensator current, placing increased

demands on the filter design.

In contrast, the NC-SVC is inherently a three phase topology, but it can still generate positive and negative sequence fundamental by modulating the firing angle with a 2^{nd} harmonic signal. This is illustrated by taking the test configuration, discussed in section 5.2 (i.e. 8.7% negative sequence voltage is added to the supply and the compensator has a constant firing angle), and adding a modulation term to the firing angle such that $\alpha = 87.7 + \varepsilon \sin(2\omega t)$.

Simulation shows that the firing angle modulation produces the same frequency of oscillation on the dc voltage and dc current. The combination of 2^{nd} harmonic on the dc current and 2^{nd} harmonic on the firing angle command produces negative sequence fundamental in the compensator current that has magnitude approximately proportional to the modulation magnitude (ε). The modulation also cancels the third harmonic positive sequence current that results from the crossmodulation, as shown in figures 5-6 and 5-7, where the levels are specified relative to positive sequence fundamental (P.S.F.). This harmonic reaches a minimum when ε is approximately 14°, but a consequence of the modulation is the production of all odd harmonic orders, as shown in figure 5-7. Of particular concern is the steady increase in negative sequence third harmonic as the modulation magnitude is increased, as shown in figure 5-6.

The maximum modulation magnitude for the software model of the NC-SVC is approximately 20°, before commutations of the reinjection bridge overlap and there is a significant increase in ac current harmonics. In the ideal case, where there are no commutations, the modulation

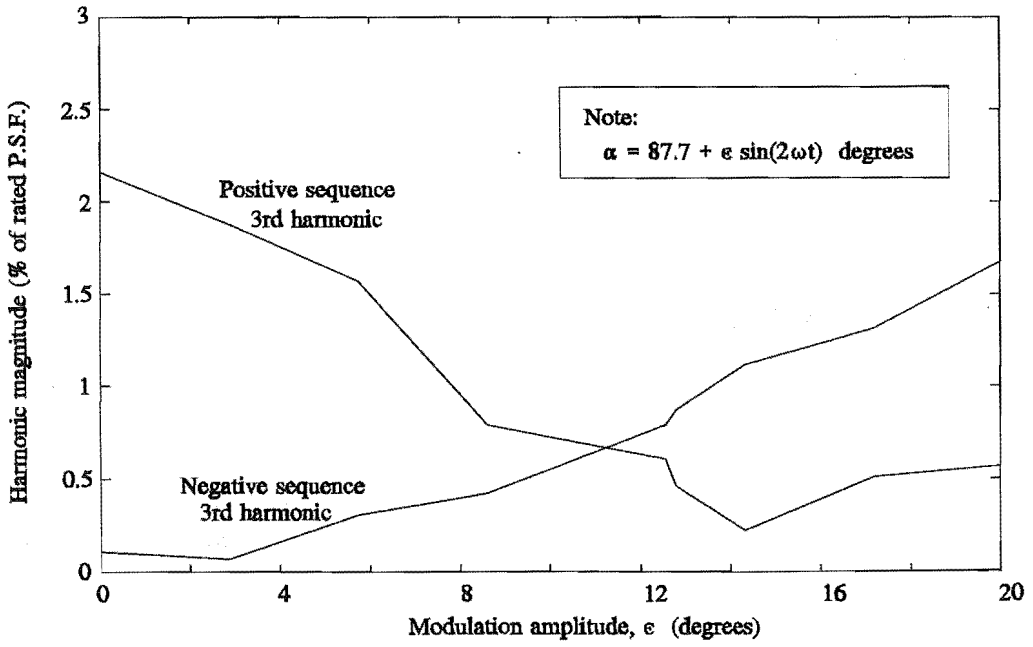

Figure 5-6: Change in third harmonic content of the ac current.

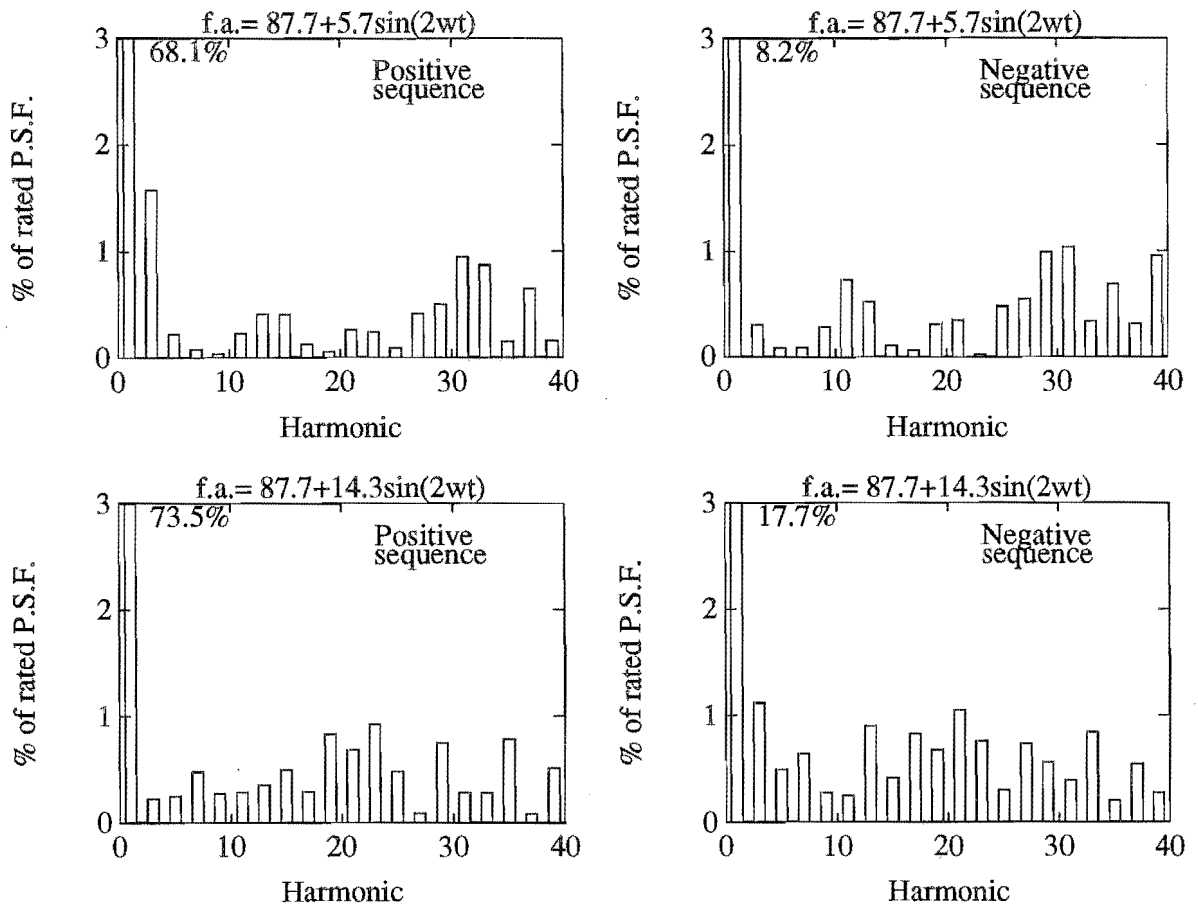

Figure 5-7: Firing angle modulation to cancel the negative sequence fundamental voltage.

magnitude can increase beyond 20°, but the nonlinearity of the convertor causes the dc current harmonics to increase, further increasing the ac current harmonics.

5.3 Dynamic operation

The duration of power system transients varies from less than a few microseconds, such as lightning and switching surges, to over 24 hours for load cycles (Miller, 1982). From the perspective of the NC-SVC, any transient that is longer than approximately one second is effectively steady state. In other words, the low frequency response of the NC-SVC is indistinguishable from any other thyristor based compensator (e.g. the TCR) with equivalent rating. Its distinguishing dynamic features (from other compensators) appear when the compensator current changes in response to ac voltage transients with duration shorter than approximately one second and these are considered in this section.

Ideally, the compensator controller, discussed in section 4.3, automatically forces the measured current to equal the current reference signal with no delay and no error. Therefore,

the interaction between the compensator and ac system is defined by the voltage control loop. Distortion in the ac voltage, however, is detected by the thyristor firing pulse synchronising feedback loop (in the controller); such distortion also modifies the current and voltage waveforms within the compensator. Furthermore, the resulting dc current distortion is detected by the current control loop.

The ac voltage transient influences all control loops described in section 4.3, potentially causing their malfunction, resulting in unexpected compensator current distortion. This issue becomes important when the compensator is trying to prevent transient instability occurring because of severe voltage disturbances. In such cases the compensator must be ready to act at the first possible instance to damp the voltage excursions. (Czech *et al.*, 1980; Muttik *et al.*, 1991 describe examples).

Transient malfunction of the NC-SVC is difficult to predict theoretically when there are nonlinear elements in the ac system and simulation is needed to demonstrate the compensators robustness. In the following sections compensator robustness is measured by exposing it to four types of ac events that produce significant levels of ac voltage deviation. A 12-pulse thyristor controlled reactor is also operated in the same ac system environment and the responses are compared. This gives a frame of reference to other dynamic studies of TCRs in power system situations that are not considered in this thesis (Miller, 1982; Gyugyi *et al.*, 1980).

5.3.1 Ac system modelling

The test system introduced in section 4.5 is used in the following simulations, except that the Thevenin equivalent (representing the utility supply) is modified to improve its frequency response and increase the number of system contingencies. The test system, which is shown in figure 5-8, is of a radial type with two buses. A Thevenin equivalent is placed at the sending bus, which is connected to the receiving bus via two parallel transmission lines each 200 km long. The load and SVC are still connected to the same bus (now called the receiving bus) so that the SVC can compensate for reactive power variations, and hence is able to control the bus voltage.

As discussed in section 4.5, the VAr capacitor banks are connected directly to the high voltage bus. This is assuming that placing capacitors on the secondary side of the TCR transformer is not an option. Theoretically, the TCR can accommodate VAr capacitors on the TCR transformer secondary, which reduces the transformer's VA rating and losses. This option is not available for the NC-SVC, therefore it is a significant factor when considering ac system situations in which the NC-SVC is competitive against the TCR.

When both transmission lines are operational, the short circuit power at the receiving bus is

2000 MVA, causing the fixed capacitors to resonate with the supply impedance at approximately the fourth harmonic. The damping of this resonance is dominated by the magnitude of the impedance type load (IEEE std-399, 1980), which is nominally set to 100 MW, 0.93 power factor in these simulations. This impedance representation of the load is valid for a variety of motor, lighting and heating loads (Pileggi *et al.*, 1981; Arrillaga *et al.*, 1990). Such a model ignores any electro-mechanical dynamics of the motors in the sub-second simulation interval, leaving only the frequency dependence to be considered. It is also assumed that there are no nonlinear loads (e.g. convertors).

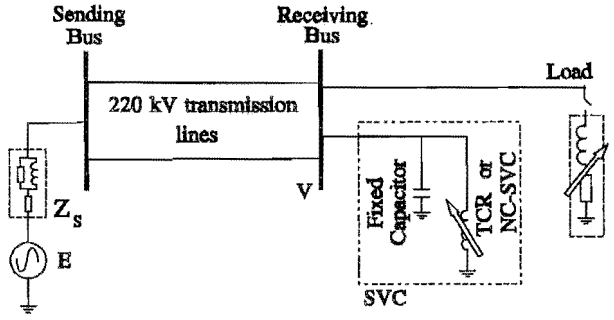

Figure 5-8: The test system

5.3.2 Thyristor controlled reactor modelling

A 12-pulse thyristor controlled reactor (TCR), with the same equivalent steady state ratings as the NC-SVC, is implemented utilising the default model from the EMTDC-PSCAD library (see Appendix D). This model incorporates VAr capacitors on the secondary side of its transformer, but to be consistent with the test configuration discussed in section 5.3.1, the rating of these capacitors are minimised. They cannot be eliminated because this causes the model to malfunction.

For the comparison of the TCR and NC-SVC topologies to be valid, the control structures must be equivalent. As discussed in section 4.3, the control structure for the NC-SVC is a nested three loop structure. The outer loop, being the voltage control loop, is independent of the circuit topology and is identical in both schemes. The power circuit for the TCR and NC-SVC, however, have different transfer functions and each current controller (i.e. a PI structure) is implemented with different parameters. Unlike the NC-SVC, the TCR has a nonlinear relationship between the firing angle and compensator susceptance, which results in a different control loop response depending on its operating point. This nonlinearity is minimised with the addition of a linearising function to the controller. To make the control

loops equivalent, the controller gains for each compensator were chosen to give similar critically damped response.

5.3.3 Dynamic situations

The dynamic compensator-system interaction is illustrated with four ac system events that cause a significant transient in the ac voltage. They include extreme overvoltage, load change, single phase to ground fault and three phase to ground fault. In each situation the power system is operated with either the TCR, the NC-SVC, or without automatic compensation; the shunt capacitor is kept in the latter case and the voltage source adjusted to provide the same initial operating point.

In all simulations the receiving bus voltage measured for the controller is passed through a low pass filter with 10 ms time constant, to produce a dc value that is indicative of the positive sequence fundamental voltage magnitude. For a given ac system event, the three ac voltage oscillograms from the three compensators are superimposed on the same plot to illustrate the relative performance of each compensator. Moreover, a current plot is shown in the figures for both the TCR and NC-SVC, with the corresponding current reference signal superimposed on the measured current; the latter taken directly from the respective compensator controllers. These current plots illustrate how well the TCR and NC-SVC maintain their operating point as specified by the AVR.

5.3.3.1 Change in ac load

The compensators steady state rating is chosen so that the compensator current remains variable in all possible variations in load level. An extreme event is a large step change in load, such as those produced by large motors or arc furnaces (Hauth *et al.*, 1982). With the load model initially set to 100 MW, a load rejection is illustrated by opening the load circuit breakers after 1 second of simulation. This causes an overvoltage condition, as shown in figure 5-9, which in the absence of automatic compensation reaches a new steady level of 1.03 pu.

After a delay of approximately 5 ms the AVRs in both compensator cases respond to the load change and increase their outputs (i.e. the current reference signals; I_{ref} shown in figure 4-7). From the time the current reference signal begins to change, the new operating level for each SVC (the 90% level) is reached in 39 and 24 ms for the TCR and NC-SVC, respectively. The difference in response time (15 ms) is confirmed when the voltage plots for the TCR and NC-SVC are compared.

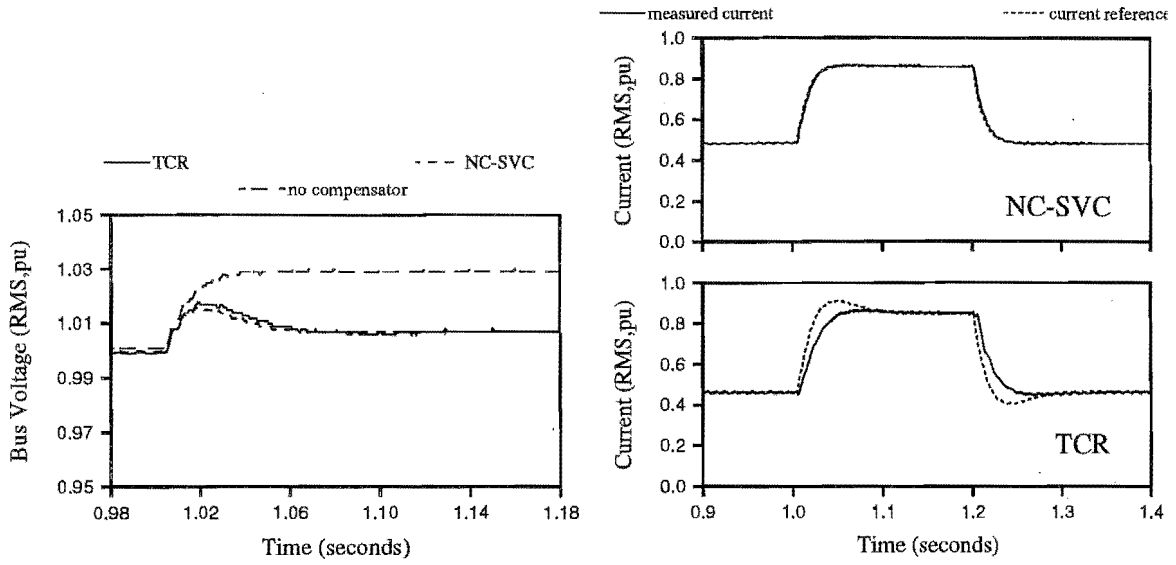

Figure 5-9: Load change at the receiving bus.

At 1.2 seconds the original load is reconnected, and the current waveforms in figure 5-9 show that the rise and fall times are symmetrical for each compensator. Moreover, the NC-SVC response time is approximately 70% that of the TCR. To check the validity of these response times, Hauth *et al.* (1978) reports a TCR response time of 1.5 cycles and Frank *et al.*(1981) reports 2 cycles, both similar to the above results.

Since the current control loops of both compensators are of equivalent structure and complexity, it is suggested that the faster response is due to the higher pulse number. This reduces the delays in compensator switching actions and a faster current controller can be designed without compromising the damping factor.

5.3.3.2 Extreme levels of overvoltage

The specification for maximum absorption of reactive current by a TCR or NC-SVC depends on the level of compensation needed in the worst case fundamental frequency overvoltage. The rarity and brevity of these extreme cases (before other slower ac system controlling mechanisms can act) means that the steady state VAr rating can be significantly smaller than the maximum VArs required, creating temporary overload capability. This relies on the components in the compensator possessing suitable thermal lags before their temperature limits are reached.

For the TCR, one limiting factor for the maximum continuously controllable VAr capability is the level of compensator current harmonics in the normal operating range (Ainsworth *et al.* 1980), as shown in figure 5-10(a) using theoretical values. With a fixed steady state VAr

rating, an increase in maximum overload effectively reduces the maximum steady state conduction angle and increases the compensator current harmonic content with respect to the rated current. In contrast, the level of overload capability in the NC-SVC changes the characteristic harmonics (i.e. 36±1), but the changes in the 12±1 and 24±1 harmonics are minor, as shown in figure 5-10(b). In other words, inherent overload capability present in the software model of the NC-SVC does not compromise the magnitudes of its 12-pulse related harmonics. This gives the NC-SVC an advantage when an overload capability is required.

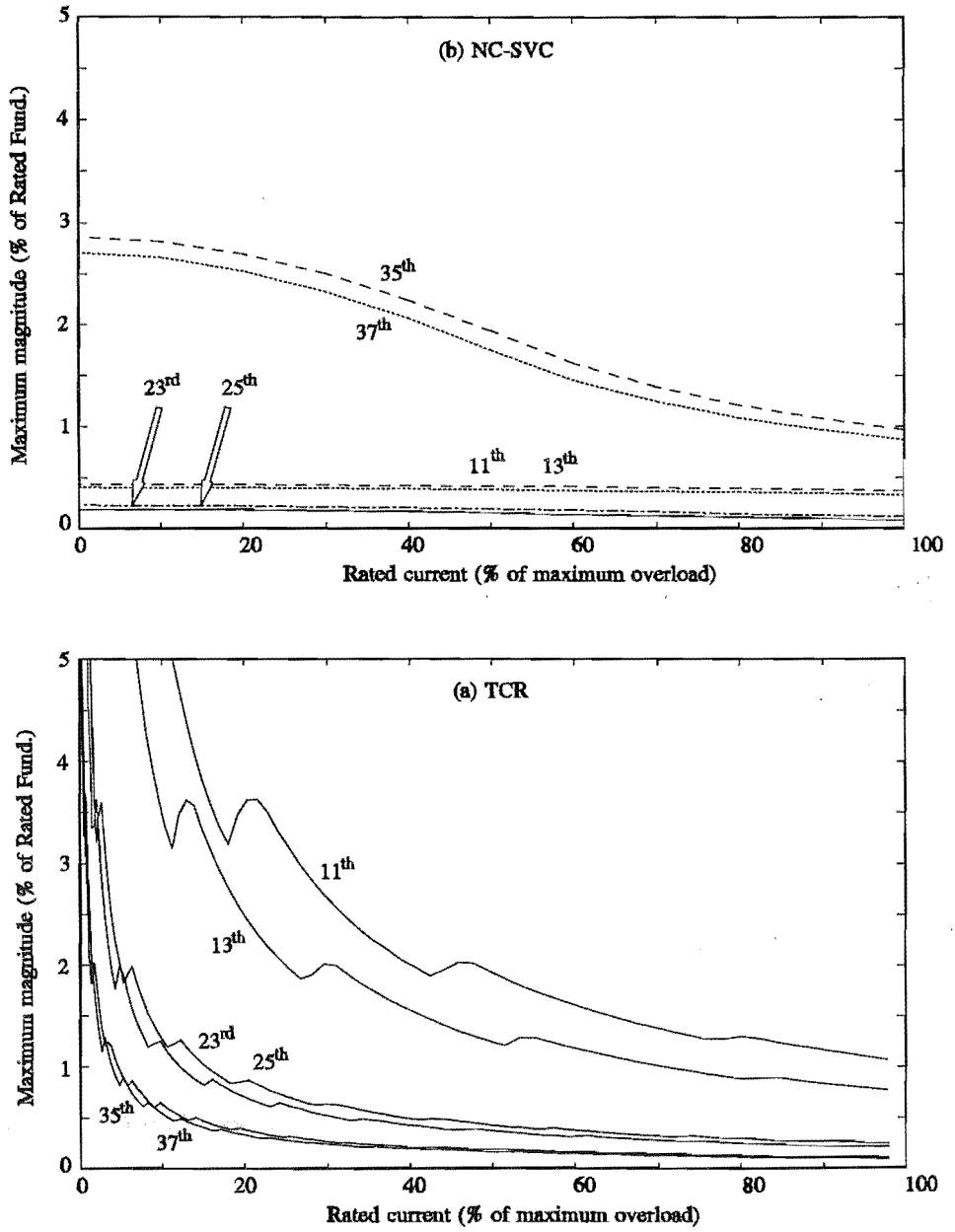

Figure 5-10: Maximum levels of ac current harmonics in the rated operating range, (a) NC-SVC and (b) TCR

The first illustration of extreme overvoltage is produced by controlling the magnitude of the ac voltage source (E) with a low frequency oscillatory characteristic, as shown in figure 5-11. Starting 1.0 second after the simulation is initiated, the voltage change is detected by the AVR in each compensator case and the compensating current increases according to the voltage control characteristic shown in figure 4-8. As defined by this characteristic, when the voltage reaches 1.01 pu the NC-SVC enters its temporary overload operating region and continues to exercise ac voltage control throughout the overvoltage condition. At approximately 1.3 seconds the NC-SVC current reaches a maximum of 1.8 pu. At 1.15 seconds the TCR reaches full conduction, corresponding to an ac voltage of 1.01 pu. The current reference signal continues to rise, but has no effect. While the ac voltage is above 1.01 pu automatic controllability of the ac voltage is lost and is not regained until the bus voltage falls below this level again. The maximum receiving bus voltages during the overvoltage condition are 1.03, 1.07 and 1.12 pu for the NC-SVC, TCR and no compensator cases, respectively.

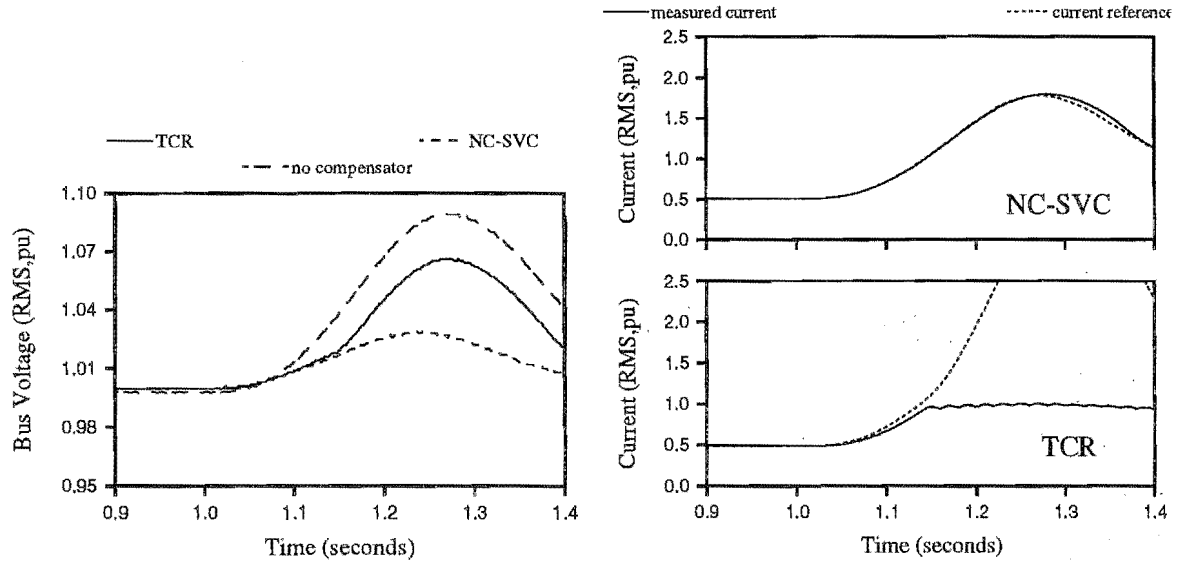

Figure 5-11: Temporary overvoltage.

For the second overload condition the voltage source (E) is held at a fixed value and a shunt capacitance and switchable inductance, both valued at 200 MVArs, are added to the receiving bus. When the inductance is temporarily removed the ac voltage suddenly increases. This situation emulates an event where VAr capacitors are left connected after a load is removed. For example, HVDC convertors typically have substantial VAr capacitor at their ac terminals that are left connected when the convertor is blocked (examples are described in Hauth *et al.*, 1982; Dabbs *et al.*, 1985; Nayak *et al.*, 1994). This contingency is anticipated and a signal is transmitted from the controlling mechanism of the inductance to the SVC. This signal is

used as an auxiliary signal within its controller, being added directly to the current reference signal, thus avoiding the delays in the voltage controller.

These events are illustrated in figure 5-12, starting with the inductance being removed at 1.0 seconds. Without compensation the ac voltage increases to 1.084 pu, but with either compensator present the ac voltage change and auxiliary signal are detected, causing the current reference signal to quickly increase. For the TCR the current is limited to 1.0 pu, corresponding to the ac voltage reaching a maximum of 1.07 pu. In the case of the NC-SVC the current is not limited, it changes to a value specified by the voltage control characteristic and the ac voltage reaches a maximum of 1.03. In both cases there is no voltage overshoot before the new steady state level is reached as is the case in section 5.3.3.1.

At 1.2 seconds the inductance is reconnected cancelling the effects of the extra capacitance. The ac voltage change and auxiliary signal are detected and the currents are forced to the same levels as at the simulation start. The sudden change in ac voltage level, however, excites the predominant resonance in the system, ie. between the fixed capacitor and supply reactance, and saturation of the compensator transformer (parameters for the EMTDC-PSCAD saturation function are listed in Appendix B). The latter occurs because a flux offset causes it to saturate in one polarity only, thus large amounts of dc and 2nd harmonic current are produced. The resulting harmonic voltages cause compensator current distortion as discussed in section 5.2. From figure 5-12, the predominantly fundamental frequency oscillation on the voltage and current plots indicates that saturation is the dominant cause of distortion.

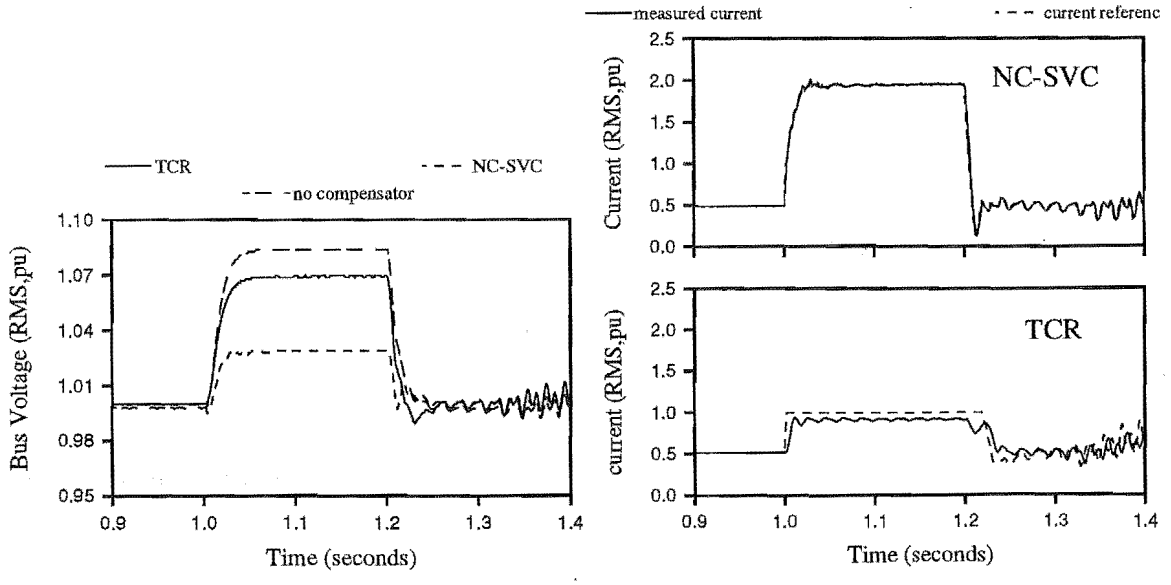

Figure 5-12: An auxiliary signal warning of a sudden voltage rise.

5.3.3.3 Single phase fault

A fault electrically close to the receiving bus and with low impedance causes a severe decrease in fundamental ac voltage and any compensation by the SVC is negligible. Moreover, it is likely that the nonideal voltage will cause the SVC to malfunction. Once the fault is cleared, however, the SVC must be ready to regulate the voltage, to control problems such as temporary overvoltage.

The single phase to ground fault is one of two fault contingencies tested in this chapter, three phase faults are discussed in section 5.3.3.4. A low impedance single phase to ground fault is applied to the receiving bus at 1.0 seconds for a 50 ms duration. During this time the RMS voltage decreases, as shown in figure 5-13. The NC-SVC current plot shows that during the fault the measured compensator current (i.e. the dc current) periodically rises above zero, which indicates abnormal convertor operation. For the TCR, the measured current includes high levels of zero sequence fundamental that circulates in the delta winding of the grounded star-delta transformer (GEC, 1987) without flowing in the thyristor/inductor branches.

In the two simulations containing compensators, the clearing of the fault causes the bus voltage to initially rise above the prefault level, due to the shunt capacitor, before the SVC control can respond. It is approximately 28 ms after the fault recovery that the compensator AVR begins to increase the current reference signals in response. This delay is the result of the linear characteristic of the controller. In actual TCR installations this delay is avoided by utilising auxiliary control algorithms that bypass the linear regulator when low voltage is detected. Typically, the compensator is forced to full conduction in preparation for the post fault operation (Hauth *et al.*, 1982). There is a further 7 ms delay before the measured

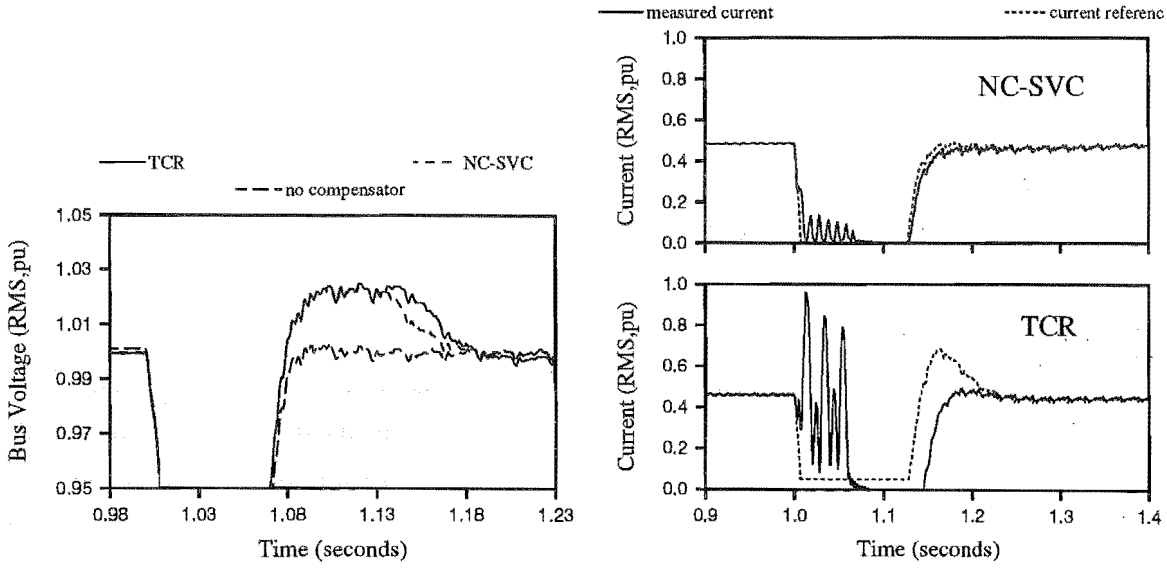

Figure 5-13: Single phase to ground fault at the receiving bus.

NC-SVC current begins to increase and for the TCR the delay is 17 ms. Again, as shown by the voltage waveforms, there is a slightly faster recovery for the NC-SVC case, due, as indicated earlier, to the higher switching frequency as compared with the TCR case.

5.3.3.4 Three phase fault

As discussed in section 5.3.3.3, SVCs are ineffective during nearby faults that cause a severe decrease in ac voltage, but the compensator must be ready to act once the fault is cleared. To test the compensator's operational readiness after a three phase fault, two situations are considered that are distinguished by the distance of the fault from the compensator.

The first fault situation is a low impedance three phase to ground fault applied to the receiving bus for 50 ms and the results are shown in figure 5-14. The fault starts at 1.0 second and all the phase voltages collapse to zero. The AVR sends the current reference signal to zero, but both the TCR and NC-SVC currents remain almost constant at the prefault level, with only a small decay. This is because the fault forms a low loss freewheeling path for the inductances in the SVCs (other examples of freewheeling are shown in Gyugyi *et al.*, 1980; Tyll *et al.*, 1993).

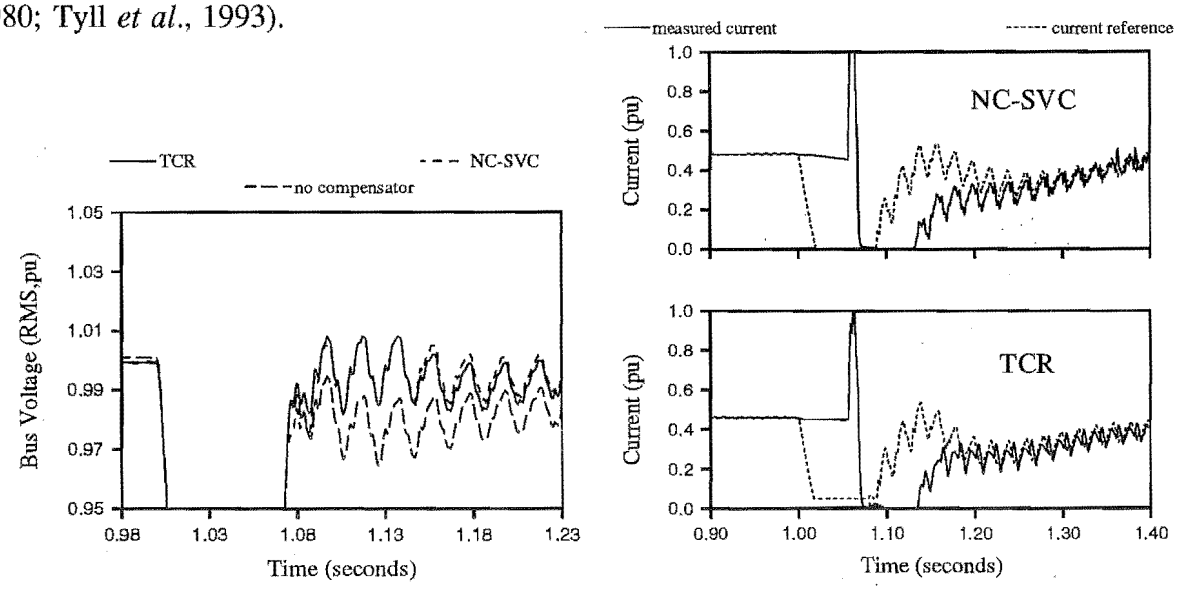

Figure 5-14: Three phase fault at the receiving bus.

When the fault is cleared the sudden application of voltage to the receiving bus causes voltage distortion because of resonance and transformer saturation, as discussed in section 5.3.3.2. The resulting harmonic voltages cause compensator current distortion as discussed in section 5.2, but the waveforms show that the these events are damped and do not cause a harmonic instability problem. Furthermore, as soon as the fault is cleared the thyristor firing pulse synchronisation loop and current control loop are attempting to resume correct operation, but

this does not happen for approximately 40 ms. Again, the linear characteristic of the controller is responsible for the degraded response. During the fault the integrator portion of the current controller steadily increases in value (ie. increasing the firing angle) in an attempt to decrease the measured current, which is impossible. When the fault is cleared the controller forces the convertor into inversion and it remains there until the integrator value reverts to normal values, the duration of this period being dictated by the integrator time constant. As mentioned in sections 4.3 and 5.3.3.2 these long delays are often avoided in actual SVC installations by including auxiliary control algorithms to bypass the linear controller.

The second three phase fault that is applied to the test system is located at the centre of one of the two transmission lines. The fault initiates at 1.0 second immediately decreasing the receiving bus voltage significantly, as shown in figure 5-15. Unlike the previous fault there

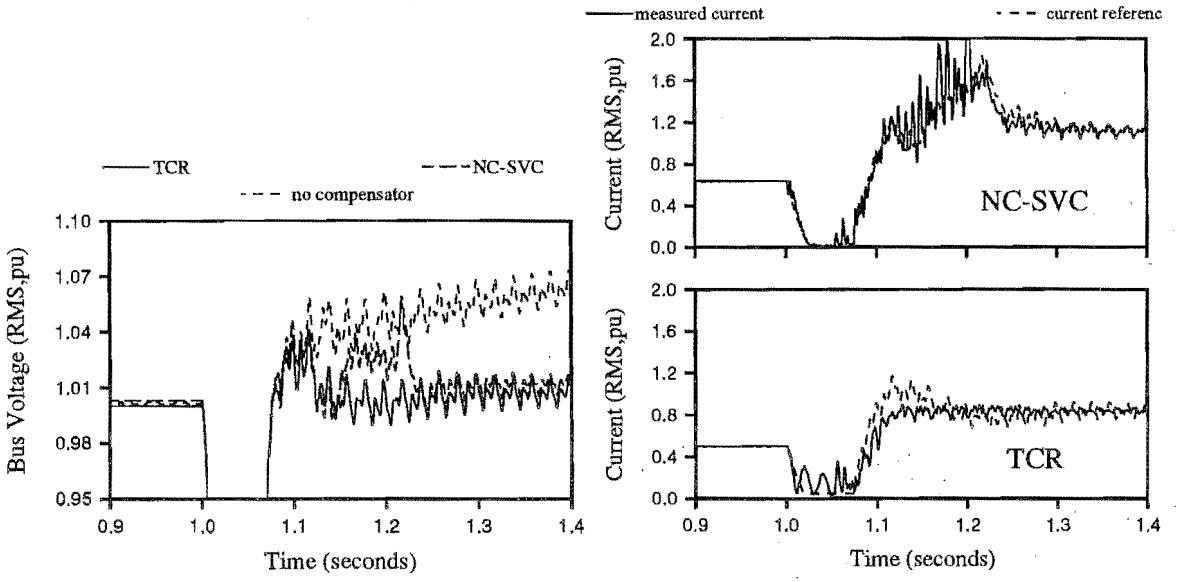

Figure 5-15: Three phase fault causing a transmission line and load trip.

is adequate ac voltage at the receiving bus, because of the other transmission line, to allow the compensators to continue to operate correctly. Once the voltage decrease is detected by the AVR, the current reference signal, in both compensator cases, is quickly lowered and the measured current follows suit.

During the fault condition the load breakers trip leaving the receiving end of the radial line unloaded. The removal of the faulted line from service at 1.05 seconds allows the ac voltage to immediately rise. In the absence of automatic compensators the voltage increases to approximately 1.07 because VAr capacitors are still connected without the load present. Approximately 24 milliseconds after the fault is cleared the AVRs begin to increase the current reference signal and both the NC-SVC and TCR are fully operational again after a further 34 and 42 ms delay, respectively. The loss of the load, however, causes an overvoltage

condition that forces the TCR to maximum current and the NC-SVC to approximately 1.2 pu. The loss of the transmission line decreases the supply-VAr capacitor resonant frequency to approximately 100 Hz, which is within the control bandwidth of the NC-SVC. This effect combined with saturation of the compensator transformer causes significant levels of low frequency distortion and the NC-SVC firing angle oscillates significantly over a period of approximately 100 ms causing malfunction. Once the distortion decays, however, the malfunction ceases and voltage control is regained.

5.4 Conclusion

In this chapter the software model of the proposed compensator is subjected to various steady state and dynamic power system conditions, and at all times the compensator current maintains the 36-pulse characteristic. The 35^{th} and 37^{th} harmonic orders exceed the two harmonic standards selected as a benchmark and the harmonic elimination required for compliance is similar to that required for the 12-pulse thyristor controlled reactor.

Using a variety of ac system events that cause significant ac voltage disturbance, the proposed scheme is shown to be consistently stable and faster at controlling the ac voltage than the TCR. Faster control is attributed to the proposed compensator's high pulse operation, allowing the current controller design to have a higher frequency response than the TCR. The larger control bandwidth, and the controller design assumption that ac voltage distortion does not effect the compensator operation means that there is a higher chance of low frequency ac voltage distortion adversely effecting the compensator operation.

Outside the frequency region where ac voltage distortion causes malfunction, the controller detects the presence of ac voltage distortion and changes the firing angle such that these voltage components are attenuated. A similar response occurs for fundamental frequency unbalance. Furthermore, it is shown that the compensator can be specifically controlled to compensate for negative sequence fundamental voltage. This is at the expense of generating current harmonics at all orders. Negative sequence compensation and operation with low distortion current are therefore mutually exclusive.

The operating condition at which the proposed scheme excels as compared to the TCR is its inherent overload capability. The NC-SVCs harmonic profile shows that its inherent overload capability, in this case approximately 4 pu, does not significantly compromise the harmonic levels, whereas the TCR overload can only be provided at the expense of considerable ac current distortion.

Chapter 6

Conclusions

As ac power systems develop there are increased economic and operational demands, requiring components such as static VAr compensators (SVC). Hence, the search for new SVC topologies that provide economic advantages and/or improved technical performance over currently available technology is ongoing. The maturity and economy of thyristor devices compared to the newer forced commutated alternatives is the reason for continued interest in thyristor based topologies. The work described in this thesis has shown that a high pulse naturally commutated SVC (NC-SVC) has the ability to absorb reactive power in a controllable manner. A dc ripple reinjection scheme has been used to provide 36-pulse operation.

Comparison of the NC-SVC with currently available technology is categorised into issues of cost and operating performance, with emphasis on the latter. The 12-pulse thyristor controlled reactor (TCR) has been used for the comparison because it is widely used in high voltage systems where low harmonic distortion is required without the need for tuned ac filters to eliminate the low order harmonics, as proposed by the NC-SVC.

Steady state and dynamic operating characteristics are considered with the help of two modelling techniques; a scaled down physical model and a full scale computer simulation using the package EMTDC-PSCAD. The results from these models show that the most important performance difference between the two topologies is the proposed scheme's superior temporary overload capability, an important attribute in many SVC applications.

The principal ratings of the components in the NC-SVC and TCR alternatives have been derived and cost comparisons made assuming that component costs are proportional to ratings. This preliminary estimate shows that the cost of the proposed scheme is similar to that of a

12-pulse thyristor controlled reactor. However, a more comprehensive quantitative assessment is left for future work.

6.1 Operating performance

Both the software and hardware models confirm that the 36-pulse ac/dc conversion process within the compensator is consistently maintained in a variety of ac system conditions. However, the characteristic harmonics of the proposed scheme exceed the harmonic limits of typical standards and further harmonic reduction is needed. Some 12-pulse related harmonics are also present because the pulse multiplication carried out by the reinjection scheme is approximate, but their levels are significantly smaller than those of the characteristic orders. Similarly, for the 12-pulse TCR, the requirement to keep the low harmonic content down inhibits the proposed scheme's ability to compensate for negative sequence unbalance on the ac voltage. The generation of negative sequence current by firing angle control results in a proliferation of harmonics of different orders.

The reactive current varies linearly with firing angle, up to in excess of 95% of the possible current range. The commutation process is the dominant factor limiting the current level in the 5% of the current range where commutation overlap occurs, eventually causing an effective short circuit at the main transformer secondary. In the case of the software model the rated current is approximately 25% of the short circuit current. Hence, it is possible to temporarily exceed the rated current by approximately 300%, constituting a significant inherent temporary overload capability. The choice of rated current with respect to the short circuit level determines the levels of characteristic harmonics in the steady state operating region, whereas the 12-pulse related harmonics are effectively independent of current level. Similarly, in the 12-pulse TCR a compromise needs to be made between overload capability and the 12-pulse related harmonic content. The ac filter requirements to eliminate 12-pulse related harmonics, however, are significantly higher than for the 36-pulse orders. Therefore, the overload levels present in the NC-SVC are not viable for the TCR.

In the dynamic situations tested, the NC-SVC is consistently faster than the TCR at controlling reactive current and ac voltage, an advantage which is attributed to its higher pulse number.

6.2 Future work

In order that the general principles of the compensator's operating performance could be identified for this thesis, several simplifying assumptions were made and they should be the target for further work.

With respect to steady state operation, the analysis describing the duration of the reinjection bridge commutation assumes that the blocking capacitor has no effect. This is not the case when the capacitor size is specified by the criteria described in chapter 2 and the analysis will need to be extended to include the capacitor. As a consequence, this analysis could be used to develop a criteria to minimise the levels of low order harmonics in the compensator current by adjusting the duration of the reinjection bridge commutation relative to the main convertor.

The software model uses a reinjection transformer representation without saturation, assuming that an actual unit would be designed to avoid that possibility. Hence, the natural resonance between the blocking capacitor and reinjection transformer magnetising inductance occurs at a single frequency. The need to understand the effect of reinjection transformer saturation on the LC resonance is two fold; how will saturation affect the damping and frequency of the oscillation and what conditions may cause ferroresonance.

Another limitation of the present software model is the use of a simple linear control algorithm. Such a scheme is far from optimal and better dynamic performance should be possible. The search for the optimal control structure is likely to involve nonlinear algorithms, which can allow for the presence of significant nonlinearity in the compensator's ac/dc conversion response. Such improvements are likely to be significant when the slow response of the voltage controller is bypassed with fast changing auxiliary signals.

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Appendix A

Component ratings for the hardware model

The scaled down hardware model of the high pulse naturally commutated SVC has a reactive power rating of 2.6 kVAr, as described in chapter 3. It is designed using criteria derived when considering the compensator's ideal operation, as discussed in chapter 2. The model is used to illustrate steady state operation and to validate the software model, discussed in chapter 4. For the latter, the hardware model is duplicated in the PSCAD-EMTDC simulation package, using component ratings listed in this appendix. These ratings are listed in the form they are entered in EMTDC-PSCAD. The impedance values are measured at 50 Hz unless otherwise stated.

Main transformer

This three phase transformer contains a star primary and two secondaries (star and delta).

Total VA rating:	2600 VA
Star primary-star secondary reactance:	0.045 pu
Star primary-delta secondary reactance:	0.023 pu
Star secondary-delta secondary reactance:	0.055 pu

Main transformer winding data

	voltage (V; ph-ph)	Resistance (Ω)
Star primary	312	0.19
Star secondary	75.7	0.052
Delta secondary	79.1	0.027

Magnetising current harmonics at rated voltage.

Harmonic	1	3	5	7	9	11	15
Harmonic magnitude (% of rated)	4.6	3.3	1.3	0.45	1.7	0.38	0.27

Reinjection transformer

The two single phase reinjection transformers are of identical construction. The magnitude of the magnetising current at rated voltage is 4.9% of rated current. Other parameters are:

VA rating: 210 VA

leakage reactance: 0.012 pu

Reinjection transformer winding data

	Voltage (V)	added resistance (Ω)
Primary winding (main bridge side)	31.6	0.07
Secondary winding (reinj. bridge side)	20.9	0.04

Thyristors

type: FCR 81 U08

main bridge snubbers: R=120Ω, C=0.22μF

reinjection bridge snubbers: R=390Ω, C=0.22μF

Ac generator and cabling

The ac generator and cabling to the hardware model is represented as a voltage source (312

V ph-ph) in series with an impedance. The impedance consists of a resistance 2.2 Ω in series with a parallel combination of an inductive reactance (2 Ω) and resistance (70 Ω).

Impedances

The ac reactor added in series with the main transformer primary is formed on an iron core with air gap and its impedance is 0.68 + j3.4 Ω. The dc reactor has a gapless iron core, its inductance is 2.8 mH and resistance is 0.07 Ω.

Two equivalent banks of blocking capacitors consist of electrolytic and ac capacitors. At 300 Hz these capacitor banks have a capacitance value of 1500μF in series with a resistance of 0.15 Ω.

Appendix B

Component ratings for the software model

The high pulse naturally commutated SVC is best suited for high voltage ac transmission systems, where the compensator ratings are in the MVAr range. To test the steady state and dynamic performance in this application a 100 MVAr software model is implemented in EMTDC-PSCAD, as described in chapter 4. It is designed using criteria derived from the compensator's ideal waveforms, as described in chapter 3. The ratings are listed in this appendix in the form needed for direct entry into the software package. Impedances are specified at 50 Hz unless otherwise stated.

Main transformer

This three phase transformer contains a star primary and two secondaries (star and delta).

VA rating:	100 MVA
leakage reactances	
star prim.-star sec.:	0.2 pu
star prim.-delta sec.:	0.2 pu
star sec.-delta sec.:	0.04 pu
saturation characteristic	
air core reactance:	0.2 pu
inrush decay time const.:	1.0 sec
knee voltage:	1.25 pu
time to release flux clipping:	0 sec

Main transformer winding data

	voltage (kV)	added resistance (Ω)	magnetising current (%)
primary winding	220	2.4	0.5
star secondary	25	0.03	0.5
delta secondary	25	0.03	0.5

Reinjection transformer

The two single phase reinjection transformers are identical. The following parameters are specified assuming a 50 Hz operating frequency even though it operates at 300 Hz:

VA rating	8.1 MVA
Leakage reactance	0.01 pu
saturation characteristic	NIL

Reinjection transformer winding data

	Voltage (kV)	added resistance (Ω)	magnetising current (%)
Primary winding (main bridge side)	32.4	0.06	1
Secondary winding (reinj. bridge side)	21.4	0.04	1

Thyristors

main bridge snubbers:	R=750 Ω, C=0.116 μF
reinjection bridge snubbers	
bridge:	R=300 Ω, C=0.148 μF
Shorting thyristor:	R=600 Ω, C=0.148 μF

Impedances

blocking capacitor:	582 μF
dc impedance inductance:	100 mH
dc impedance resistance:	0.03 Ω

Control

The phase lock loop, inbuilt into the Graetz bridge model, has a proportional gain of 10.0 and integral gain of 100.0.

Appendix C

220 kV transmission line data

In chapter 5 the high pulse naturally commutated SVC and thyristor controlled reactor are tested in a simple high voltage ac system. The test system is of a radial type with two buses. Generation is connected at the sending bus and the load at the receiving bus. These buses are separated by 200 km and are connected together with two parallel transmission lines. The two lines are identical, having the same tower configuration (i.e. single circuit as shown in figure C-1) and transmission line data. One line is configured such that a mid point connection is available to apply functions such as faults. This appendix lists the transmission line data in a form needed for direct entry into EMTDC-PSCAD.

The resistivity of the ground is 100.0 ohm-m.

Conductor wire data

name	ZEBRA (54/318 + 7/3.18 ACSR)
voltage (kV) (L-L RMS)	220
number of sub-conductors	1
sub-conductor radius (cm)	2.858
sub-cond spacing (cm)	0
sag at midspan (m)	2
dc resistance (ohms/km)	0.07 (i.e. ac resistance)
conductor positions	

Earth wire data

name	31 (7/3.18 GEHSS)
conductor radius (cm)	0.952
sag at midspan (m)	2
dc resistance (ohms/km)	0.07

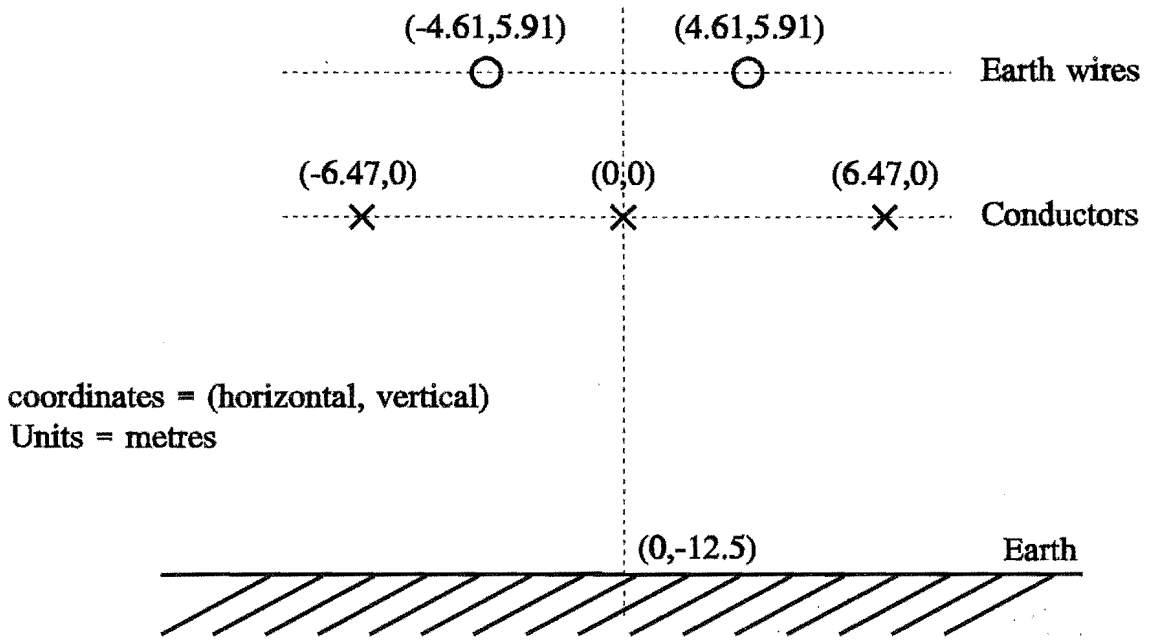

Figure C-1: Transmission line tower configuration

Appendix D

Component ratings for the thyristor controlled reactor model

Chapter 5 describes the dynamic performance of the naturally commutated SVC compared to existing technology (i.e. the 12-pulse thyristor controlled reactor). Both schemes are implemented in the EMTDC-PSCAD package with the same MVAr rating (100MVAr). Results obtained when both compensators are operated in the same power system environment and with the same control strategy are compared. The TCR is implemented using EMTDC-PSCAD's inbuilt library component and the data in this appendix. The component ratings are listed in the form they are entered in EMTDC-PSCAD.

Main three phase transformer

VA rating:	100 MVA
star primary:	220 kV
star secondary:	12.65 kV
delta secondary:	12.65 kV
magnetising current:	0.5 %
leakage reactances	
star prim.-star sec.:	0.2 pu
star prim.-delta sec.:	0.2 pu
star sec.-delta sec.:	0.04 pu
saturation	
air core reactance:	0.2
inrush decay time const.:	1.0
knee voltage:	1.25 pu

time to release flux clipping: 0

Thyristors

snubber resistance: 1000 ohms
snubber capacitance: 0.3 μF

Impedances

internal VAr capacitors: 0.5 MVAr
parallel resistance: 500 ohms
total VAr rating for the TCR: 100 MVAr

Control

The phase lock loop has a proportional gain of 10.0 and integral gain of 100.0. Unlike the NC-SVC, the TCR has a nonlinear relationship between the firing angle (α), where $\frac{\pi}{2}<\alpha<\pi$, and compensator susceptance (B_L), where $1.5>B_L>0$. The effect of the nonlinearity can be removed by modifying the firing angle command with a function that is an inverse of that nonlinearity. In this case, the nonlinearity is reduced to insignificant levels with an approximate inverse function of the form

$$\alpha = A + B \log_{10}(CB_L + D)) \qquad \text{(D-1)}$$

The coefficients A,B,C and D are calculated by restraining the values of α and B_L at the extremes of the operating region and at one mid point, resulting in the function

$$\alpha = \frac{\pi}{2}(1 + 1.24 \log_{10}(3.6B_L + 1)) \qquad \text{(D-2)}$$